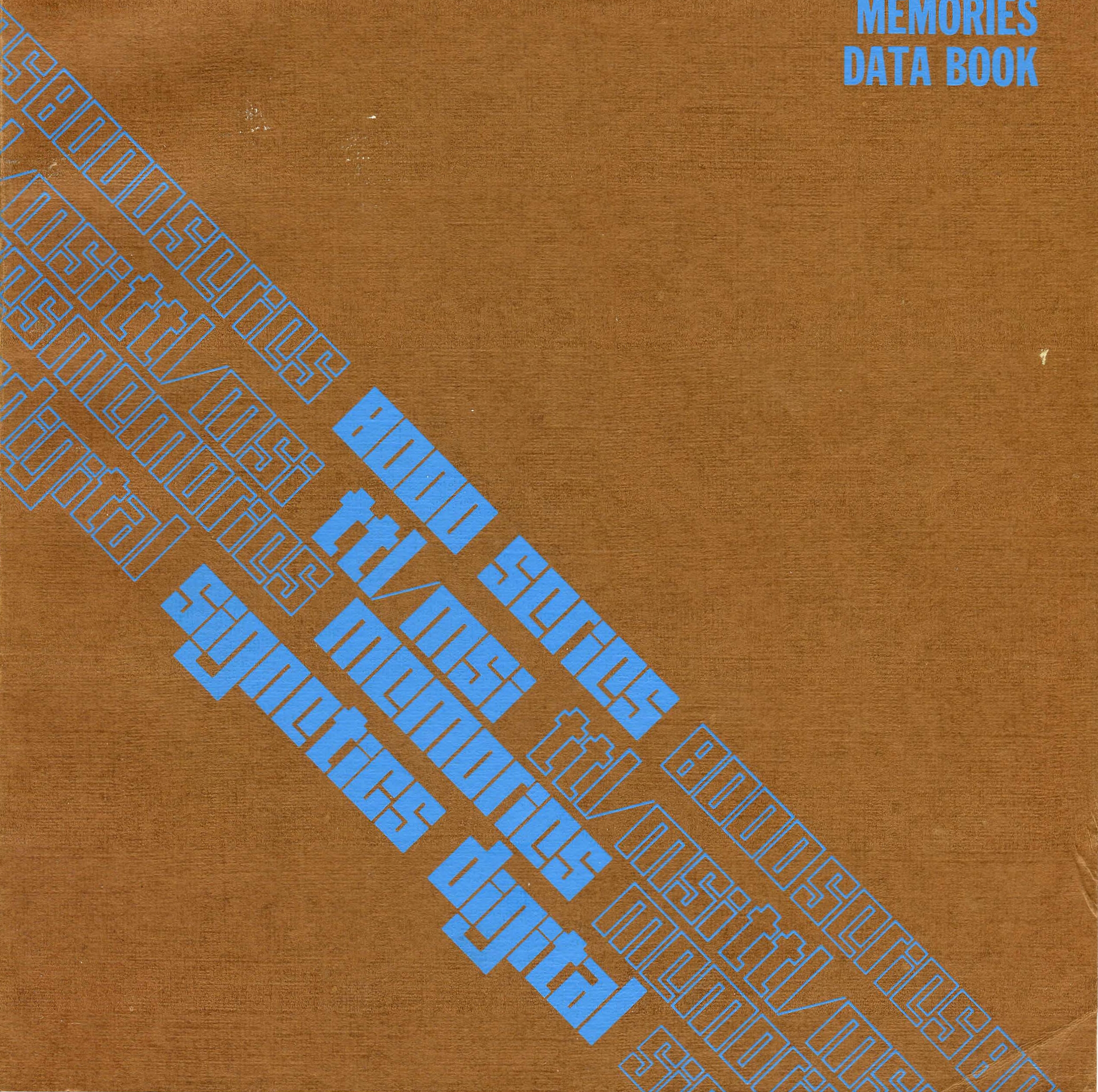
SIGNETICS
DIGITAL
8000 SERIES
TTL/MSI AND
MEMORIES
DATA BOOK



DIGITAL 8000 SERIES TTL/MSI

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SECTION 1
INTRODUCTION AND ORDER INFORMATION

INTRODUCTION

The DCL MSI (Medium Scale Integration) Specifications Handbook comprises the second volume of the DCL Series and covers the MSI group of the DCL family.

Volume one of the DCL Series includes gates, binaries and less complex functions such as monostable multivibrators and interface elements.

The material is designed to serve as an exact guide to generate a procurement document. Section 4, "Design Considerations," provides maximum ratings and package outlines for all devices listed in this volume. Section 7, "Electrical Characteristics," contains detailed test limit and test condition information for simplified device evaluation and incoming inspection. The material is organized in a format which lends itself to generation of device specifications with a minimum of cost and time. Worst case limits are provided for most parameters.

Because of the growing complexity of new DCL/MSI products, loading and noise margin tables are not included in this volume. The numbers are easily generated for individual cases as shown below. The lower of the two numbers is the DC fan-out.

DC Noise Margin ("0" state) is obtained by subtracting the maximum "0" level output voltage for the driving gate from the minimum "0" threshold for the driven gate.

DC Noise margin ("1" state) is obtained by subtracting the maximum "1" level input threshold of the driven gate from the minimum "1" output voltage level of the driving gate.

Application ideas are provided with each product data sheet. For more complete applications information, ask for Signetics' Application Handbook.

Section 8 of this volume presents the Signetics' SURE Product Assurance and Reliability programs. Production screens, acceptance tests, qualification tests, design tests and an optional HI-REL screening program specially tailored to Signetics devices are described. The applicable SURE programs, combined with individual DCL specification sheets, are designed to constitute a complete procurement document. Use of these standard specifications will provide fast and accurate specifications and product flow.

$$\text{DC FAN OUT ("0" OUTPUT CONDITION)} = \frac{\text{"0" maximum output current of driving element}}{\text{"0" maximum input current requirement of driven element}}$$

$$\text{DC FAN OUT ("1" OUTPUT CONDITION)} = \frac{\text{"1" maximum output current of driving element}}{\text{"1" maximum input current requirement of driven element}}$$

ORDER INFORMATION

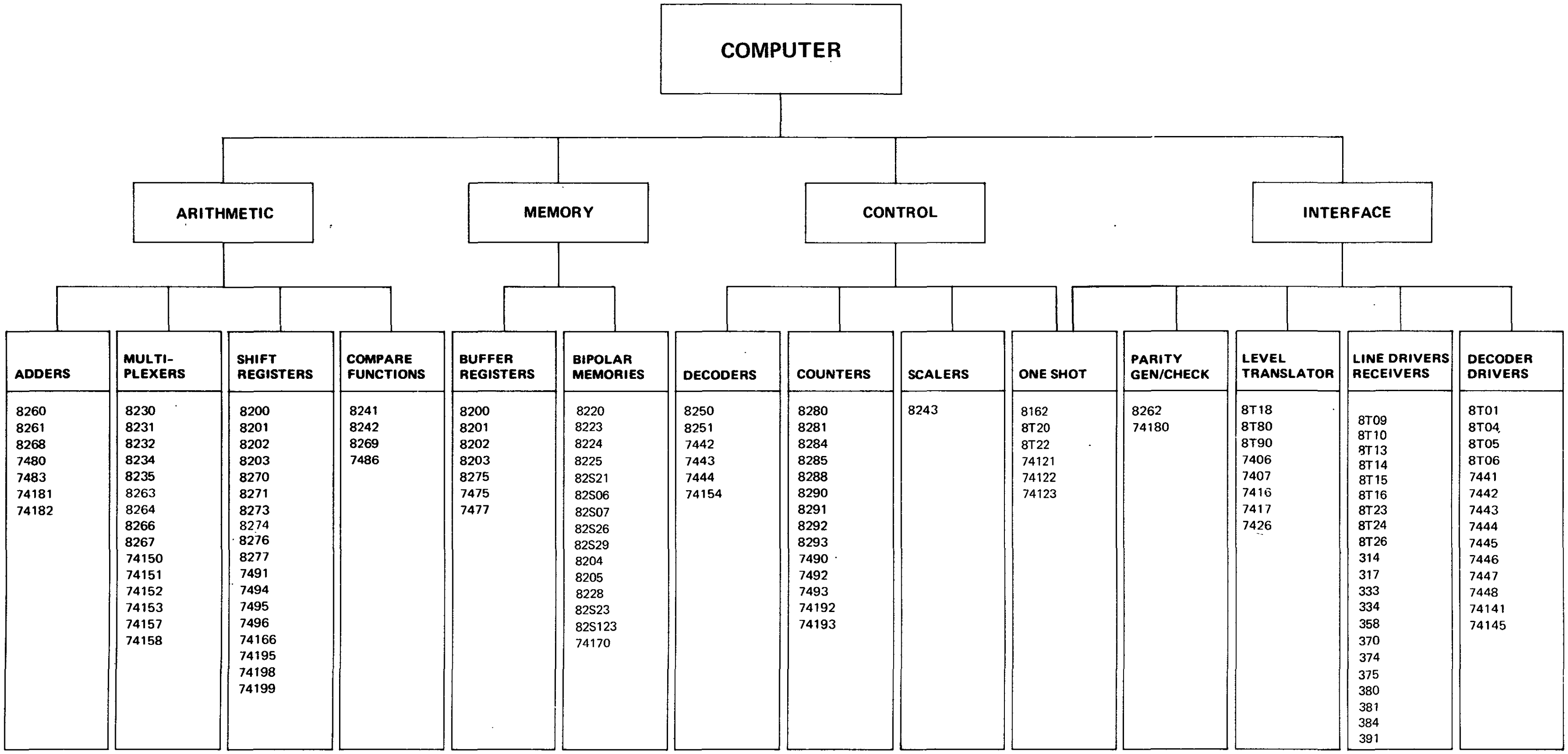
PART IDENTIFICATION
YSXXXZ

Y TEMPERATURE RANGE:

"S" = –55°C TO +125°C
"N" = 0°C TO +75°C

Z PACKAGE TYPE:

"A" = 14-PIN DUAL IN-LINE SILICON PACKAGE
"B" = 16-PIN DUAL IN-LINE SILICON PACKAGE
"N" = 24-PIN DUAL IN-LINE SILICON PACKAGE
"F" = 14, 16, 24-PIN CERDIP
"W" = 14, 16-PIN CERPAC
"I" = 16-PIN CERAMIC DUAL IN-LINE
"Q" = 24-PIN CERAMIC FLAT PAC
"YB" = 24-PIN CERAMIC DIP



ARITHMETIC				MEMORY		CONTROL				INTERFACE			
ADDERS	MULTI-PLEXERS	SHIFT REGISTERS	COMPARE FUNCTIONS	BUFFER REGISTERS	BIPOLAR MEMORIES	DECODERS	COUNTERS	SCALERS	ONE SHOT	PARITY GEN/CHECK	LEVEL TRANSLATOR	LINE DRIVERS RECEIVERS	DECODER DRIVERS
8260	8230	8200	8241	8200	8220	8250	8280	8243	8162	8262	8T18	8T09	8T01
8261	8231	8201	8242	8201	8223	8251	8281		8T20	74180	8T80	8T10	8T04
8268	8232	8202	8269	8202	8224	7442	8284		8T22		8T90	8T13	8T05
7480	8234	8203	7486	8203	8225	7443	8285		74121		7406	8T14	8T06
7483	8235	8270		8275	82S21	7444	8288		74122		7407	8T15	7441
74181	8263	8271		7475	82S06	74154	8290		74123		7416	8T16	7442
74182	8264	8273		7477	82S07		8291				7417	8T23	7443
	8266	8274			82S26		8292				7426	8T24	7444
	8267	8276			82S29		8293					8T26	7445
	74150	8277			8204		7490					314	7446
	74151	7491			8205		7492					317	7447
	74152	7494			8228		7493					333	7448
	74153	7495			82S23		74192					334	74141
	74157	7496			82S123		74193					358	74145
	74158	74166			74170							370	
		74195										374	
		74198										375	
		74199										380	
												381	
												384	
												391	

COMPUTER APPLICATIONS FOR SIGNETICS MSI AND INTERFACE ELEMENTS

(Contact your nearest Signetics Sales office for the latest TTL products)

SECTION 2
DIGITAL FAMILY LINES

The following is a parts list of Signetics Digital Product Lines, now available, as described in the UTILOGIC II, DCL, and 54/74 Handbooks.

UTILOGIC II/SP600 LINE

NOR Gates	
314A	Single 7-Input NOR Gate
317A	Dual 4-Input Expandable NOR Gate
370A	Triple 3-Input NOR Gate
380A	Quad 2-Input NOR Gate
381A	Quad 2-Input NOR Gate (Open-Collector)
OR Gates	
333A	Dual 3-Input Expandable OR Gate
334A	Dual 4-Input Expandable OR Gate
374A	Triple 3-Input OR Gate
375A	Triple 2-Input OR Gate
384A	Quad 2-Input OR Gate
AND Gates	
302A	Quad 2-Input AND Gate
304A	Dual 4-Input AND Gate (Expandable)
305A	Single 6-Input AND Gate
306A	Dual 3-Input AND Gate
NAND Gates	
337A	Dual 4-Input Expandable NAND Gate
377A	Triple 3-Input NAND Gate
387A	Quad 2-Input NAND Gate
616A	Dual 3-Input Expandable NAND Gate
670A	Triple 3-Input NAND Gate
680A	Quad 1-Input NAND Gate
Gate Expanders	
300A	Dual 3-Input Expander for OR and NOR Gates
301A	Quad 2-Input Diode Expander for NAND Gates
Buffer Drivers	
352A	Dual 3-Input Expandable NAND Buffer Driver (Open Collector)
356A	Dual 4-Input Expandable NAND Buffer Driver
357A	Quad 2-Input NAND Power Driver
358A	Quad 2-Input NAND Power Driver (Open Collector)
Binaries	
321A	Dual J-K Binary
322A	Dual J-K Binary
328A	Dual D Binary
620A	Single J-K Master Slave Binary
629A	Single RS/T Binary
Pulse Shapers	
362A	Monostable Multivibrator
Zero Crossing Detector	
363A	Dual Zero Crossing Detector
Shift Register	
3271B	4-Bit Shift Register
Counters	
3280A	BCD Decade Counter
3281A	4-Bit Binary Counter
Buffer Driver	
659A	Dual 4-Input Buffer/Driver (Expandable)
Inverter	
391A	Hex Inverter (Open Collector)
690A	Hex Inverter
Expander	
631A	Gate Expander

DCL DIGITAL LINE

Multivibrator	
8162	Monostable Multivibrator
Low Power Elements	
8415	Dual 5-Input NAND Gate
8416	Dual 4-Input Expandable NAND Gate
8417	Dual 3-Input Expandable NAND Gate
8424	Dual RS/T Binary
8425	Dual RS/T Binary
8226	1024 BIT Field/Factory Programmable Bipolar ROM (256 x 4)
8228	4096 BIT Bipolar ROM (1024 x 4)
8440	Dual AND-OR-Invert Gate
8455	Dual 4-Input NAND Gate Driver
8470	Triple 3-Input NAND Gate
8471	Triple 3-Input NAND Gate
8480	Quad 2-Input NAND Gate
8481	Quad 2-Input NAND Gate
8490	Hex Inverter
8706	Dual 5-Input Diode Expander Element
8731	Quad 2-Input Diode Expander Element
Standard Performance Elements	
8806	Dual 4-Input Expander Element
8808	Single 8-Input NAND Gate
8815	Dual 4-Input NOR Gate
8816	Dual 4-Input NAND Gate
8821	Dual Master-Slave J-K Binary
8822	Dual Master-Slave J-K Binary
8824	Dual Master-Slave J-K Binary
8825	DC Clocked J-K Binary
8826	Dual J-K Binary
8827	Dual J-K Binary
8828	Dual D Binary
8829	High Speed J-K Binary
8840	Dual Expandable AND-OR-Invert Gate
8848	Expandable AND-OR-Invert Gate
8855	Dual 4-Input Driver
8870	Triple 3-Input NAND Gate
8875	Triple 3-Input NOR Gate
8880	Quad 2-Input NAND Gate
8881	Quad 2-Input NAND Gate
8885	Quad 2-Input NOR Gate
High Speed Elements	
8H16	Dual 4-Input NAND Gate
8H20	Dual J-K Binary Element
8H21	Dual J-K Binary Element
8H22	Dual J-K Binary Element
8H70	Triple 3-Input NAND Gate
8H80	Quad 2-Input NAND Gate
8H90	Hex Inverter
Interface Elements	
8T18	Dual 2-Input NAND Interface Gate
8T80	Quad 2-Input NAND Interface Gate
8T90	Hex Inverter Interface Element

DIGITAL FAMILY LINES (Cont'd)

54/74XX - 54/74HXX LINE

54/7400	Quadruple 2-Input Positive NAND Gate
54/7401	Quadruple 2-Input Positive NAND Gate (With open collector output)
54/7402	Quadruple 2-Input Positive NOR Gate
54/7403	Quadruple 2-Input Positive NAND Gate (With open collector output)
54/7404	Hex Inverter
54/7405	Hex Inverter (With open collector output)
54/7406	Hex Inverter Buffer/Driver with Open Collector High Voltage Outputs
54/7407	Hex Buffer/Driver with Open Collector High Voltage Outputs
54/7408	Quadruple 2-Input Positive AND Gates
54/7409	Quad 2-Input AND Gate with Open Collector Outputs
54/7410	Triple 3-Input Positive NAND Gate
54/7411	Triple 3-Input Positive AND Gate
54/7416	Hex Inverter Buffer/Driver with Open Collector High Voltage Outputs
54/7417	Hex Buffer/Driver with Open Collector High Voltage Outputs
54/7420	Dual 4-Input Positive NAND Gate
54/7421	Dual 4-Input AND Gate
54/7426	Quad 2-Input High Voltage NAND Gate
54/7430	8-Input Positive NAND Gate
54/7437	Quad 2-Input NAND Buffer
54/7438	Quad 2-Input NAND Buffer
54/7440	Dual 4-Input Positive NAND Buffer
54/7442	BCD - to - Decimal Decoder
54/7443	Excess 3 - to - Decimal Decoder
54/7444	Excess 3 - Gray - to - Decimal Decoder
54/7445	BCD-to-Decimal Decoder/Driver with Open Collector High Voltage Outputs
7446/47	BCD-to-Seven Segment Decoder/Driver
7448	BCD-to-Seven Segment Decoder/Driver
54/7450	Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate
54/7451	Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate
54/7453	4-Wide 2-Input AND-OR-Invert Gate
54/7454	4-Wide 2-Input AND-OR-Invert Gate
S5460	Dual 4-Input Expander
N7460	Dual 4-Input Expander
54/7470	J-K Flip-Flop
54/7472	J-K Master-Slave Flip-Flop
54/7473	Dual J-K Master-Slave Flip-Flop
54/7474	Dual D-Type Edge-Triggered Flip-Flop
54/7475	Quadruple Bistable Latch
54/7476	Dual J-K Master-Slave Flip-Flop with Preset and Clear
54/7477	Quadruple Bistable Latch
54/7480	Gated Full Adder
54/7483	4-Bit Binary Full Adder (Look Ahead Carry)
54/7486	Quad 2-Input Exclusive OR Gate
54/7488	256-Bit Read-Only Memory
54/7489	64-Bit Read/Write Memory (RAM)
54/7490	Decade Counter
54/7491	8-Bit Shift Register
54/7492	Divide-by-Twelve Counter (Divide-by-Two and Divide-by-Six)
54/7493	4-Bit Binary Counter
54/7494	4-Bit Shift Register (Parallel-In, Serial-Out)
54/7495	4-Bit Right-Shift Left-Shift Register
54/7496	5-Bit Shift Register
54/74107	Dual J-K Master Slave Flip-Flop
54/74121	Monostable Multivibrator
54/74122	Retriggerable Monostable Multivibrator with Clear
54/74141	BCD-to-Decimal Decoder/Driver with Blanking
54/74145	BCD-to-Decimal Decoder/Driver with Open Collector High Voltage Outputs
54/74150	16-Line to 1-Line Data Selector/Multiplexer
54/74151	8-Line to 1-Line Data Selector/Multiplexer
54/74152	8-Line to 1-Line Data Selector/Multiplexer

54/74XX - 54/74HXX LINE (Cont'd)

54/74154	4-Line to 16-Line Decoder/Demultiplexer
54/74180	8-Bit Odd/Even Parity Generator/Checker
54/74192	Synchronous Decade Up/Down Counter with Preset Inputs
54/74193	Synchronous 4-Bit Binary Up/Down Counter with Preset Inputs
54/74194	4-Bit Bidirectional Universal Shift Register
54/74H00	Quadruple 2-Input Positive NAND Gate
54/74H01	Quadruple 2-Input Positive NAND Gate (With open collector output)
54/74H04	Hex Inverter
54/74H05	Hex Inverter (With open collector output)
54/74H08	Quadruple 2-Input Positive AND Gate
54/74H10	Triple 3-Input Positive NAND Gate
54/74H11	Triple 3-Input Positive AND Gate
54/74H20	Dual 4-Input Positive NAND Gate
54/74H21	Dual 4-Input Positive AND Gate
54/74H22	Dual 4-Input Positive NAND Gate (With open collector output)
54/74H30	8-Input Positive NAND Gate
54/74H40	Dual 4-Input Positive NAND Buffers
54/74H50	Dual 2-Wide 2-Input AND-OR-Invert Gates
54/74H51	Dual 2-Wide 2-Input AND-OR-Invert Gates
54/74H52	4-Wide 2-2-2-3-Input AND-OR-Gate
54/74H53	Expandable 2-2-2-3-Input AND-OR-Invert Gate
54/74H54	Expandable 2-2-2-3-Input AND-OR-Invert Gate
54/74H55	Expandable 4-Input AND-OR-Invert Gate
54/74H60	Dual 4-Input Expander (For use with S54H50, S54H53, S54H55 circuits)
54/74H60	Dual 4-Input Expander (For use with N74H50, N74H53, N74H55 circuits)
54/74H61	Triple 3-Input Expanders (For use with S54H52, N74H52 circuits)
S54H62	3-2-2-3-Input AND-OR-Expander (For use with S54H50, S54H53, S54H55 circuits)
N74H62	3-2-2-3-Input AND-OR Expander (For use with N74H50, N74H53, N74H55 circuits)
54/74H72	J-K Master Slave Flip-Flops
54/74H73	Dual J-K Master-Slave Flip-Flops
54/74H74	Dual D-Type Edge-Triggered Flip-Flops
54/74H76	Dual J-K Master-Slave Flip-Flops

NEW 54/74 PRODUCTS

54/7413	Dual NAND Schmitt Trigger
54/74123	Dual Retriggerable Monostable Multivibrator W/Clear
54/74153	Data Selector/Multiplexer Dual 4-to-1 Line
54/74157	Quadruple 2-Line to 1-Line Selector/Multiplexer
54/74158	Quadruple 2-Line to 1-Line Selector/Multiplexer
54/74160	Synchronous Counters with Direct Clear
54/74161	Synchronous Counters with Direct Clear
54/74162	Fully Synchronous Counters
54/74163	Fully Synchronous Counters
54/74166	Parallel-In, Serial-Out, Synchronous Load Shift Register
54/74170	4 x 4 Register File
54/74181	4-Bit Arithmetic Unit W/Full Look-Ahead
54/74182	Look-Ahead Carry Generator
54/74195	4-Bit Shift Register Parallel-Access J-K Inputs Mode Control
54/74198	8-Bit Shift Register Parallel-Access, Shift Right-Left
54/74199	8-Bit Shift Register Parallel-Access J-K Inputs W/Mode Control
54/74S00	Quad 2-Input NAND Schottky
54/74S112 *	Dual J-K Flip-Flop Schottky
54/74S113 *	Dual J-K Flip-Flop Schottky
54/74S114 *	Dual J-K Flip-Flop Schottky
54/74H71	J-K Master Slave Flip-Flop

* Available Soon

SECTION 3
DESIGN CONSIDERATIONS

OUTPUT STRUCTURES

Certain guidelines should be observed to ensure optimum system performance. Systems incorporating TTL elements such as gates, binaries and MSI circuits have inherent V_{CC} and GROUND transients attributable to the current spike produced by "totem pole" output structures. Figure 1 provides a synopsis of the commonly used totem pole structures which current spike. MSI designs use similar structures to buffer outputs and inputs to increase fan-out and switching speed while reducing input loading.

COMMON TOTEM POLE OUTPUT STRUCTURES

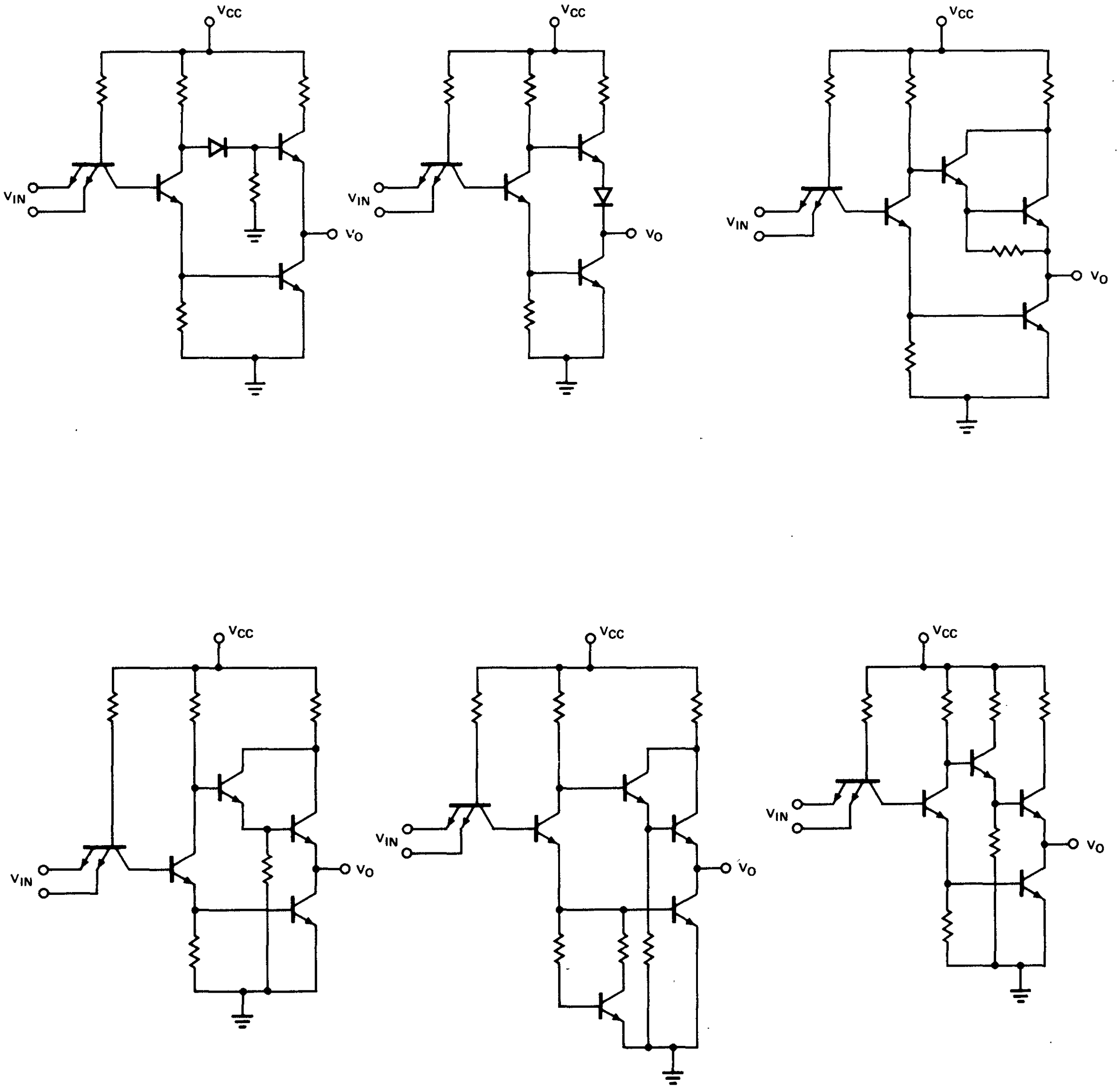


FIGURE 1

DESIGN CONSIDERATIONS (Cont'd)

DECOUPLING MSI

The current spike produced by the totem pole output structure during switching transitions can cause MSI subsystems to malfunction if V_{CC} is not adequately decoupled to GROUND. A capacitance of 2000pF or more, for each totem pole structure should be connected from V_{CC} to GROUND. The non-inductive capacitor (ceramic disc, tantalum slug, etc.) should be mounted with leads as short as possible and should be placed in close proximity to the MSI package to minimize lead length inductance. A properly designed printed circuit board should have the total required capacitance evenly distributed throughout the board. Example: A printed circuit board contains 25 packages averaging four totem pole structures per package. The total capacitance required is 25 packages x 4 totem pole structures x 2000pF or 0.2μF ceramic disc capacitors evenly distributed, satisfy the V_{CC} to GROUND decoupling requirements.

POWER SUPPLY AND GROUND DISTRIBUTION SYSTEMS

High-frequency distribution techniques should be used for V_{CC} and GROUND. These techniques should include a large ground plane to minimize DC offsets and to provide an extremely low impedance path to reduce transient voltage signals on the printed circuit board. The power supply should be +5V ±5% with R-F (1GHz) bypassing. Catastrophic damage can occur if V_{CC} is not properly regulated.

Power distributed from the main supply must, by necessity, come through a path which displays finite resistance (R_{ps}), inductance (L_{ps}) and capacitance (C_{ps}), as illustrated in Figure 2. The resistive component of the power lines is small, producing very little DC voltage drop at the V_{CC} and GROUND inputs to the printed circuit board. However, the inductance in the power lines can cause the noise generated by current spiking to be transmitted throughout the system on the V_{CC} and GROUND lines. If the printed circuit boards are adequately decoupled, the power line noise will be reduced significantly. In order to repel power line noise transmitted to a printed circuit board, ferrite beads may be placed on the incoming V_{CC} and GROUND lines as shown in Figure 3. A 10μf tantalum capacitor, per 25 packages, connected from V_{CC} to GROUND should be placed on the printed circuit board in the position shown. In conjunction with the distributed ceramic disc capacitors, this approach will prevent most system malfunctions attributable to internally generated noise.

FERRITE BEAD
ISOLATION OF GENERATED NOISE

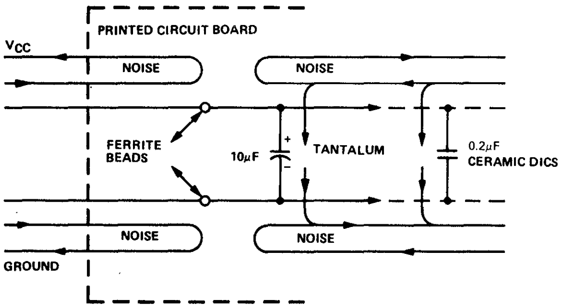


FIGURE 3

ISOLATION DIODES

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

POWER CHARACTERISTIC IMPEDANCE

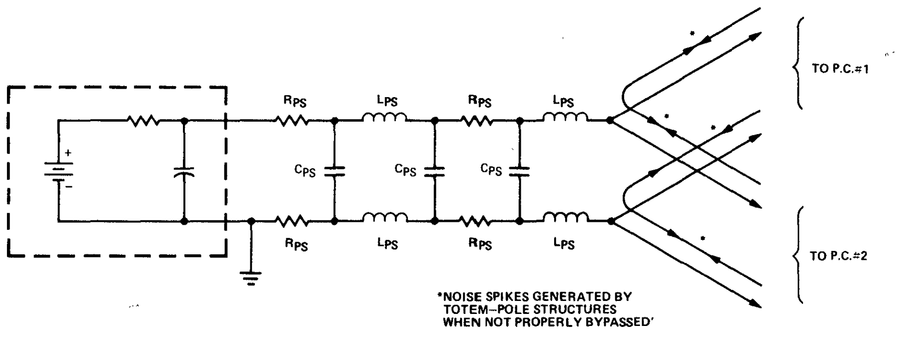


FIGURE 2

DESIGN CONSIDERATIONS (Cont'd)

DISPOSITION OF UNUSED INPUTS

Electrically open inputs degrade AC noise immunity as well as the switching speed of an MSI circuit. To optimize performance, each input must be connected to a low impedance source. Unused inputs should be tied to V_{CC}, GROUND or a driving source. When paralleling an unused input with a driven input of the same multiple emitter transistor (MET), care should be taken to remain within the "1" level fan-out specifications for the driving source. The AND or NAND structures do not affect the "0" level fan-out of the driving source. When an unused input of an OR or NOR structure is commoned with a driven input, both the "1" and "0" level fan-out of the driving source are affected.

If fan-out of the driving source will be exceeded or if there is no convenient connection to an appropriate driven input, a second method of avoiding open inputs should be observed. Inputs which activate on "0" (AND and NAND) may be tied directly to V_{CC} or tied to V_{CC} through a current limiting resistor. To determine the requirements for current limiting, examine the input "latch-back" characteristics of the MET. This check is performed by grounding all but one of the emitters of the MET. Force 10mA into the ungrounded emitter and examine the "breakdown" characteristics on a curve tracer. If "breakdown" is greater than 5.5V and there is no evidence of latch-back or secondary breakdown, an unused input may be tied directly to V_{CC}. If the breakdown voltage or latch-back characteristic approaches 5.5V at 10mA, the input should be tied to V_{CC} through a current limiting resistor of 1 KΩ or more. More than one unused input can be tied to V_{CC} through a single resistor.

The 8200 series of MSI subsystems does not exhibit a latch-back characteristic. A current limiting resistor is required, however, if power supply transients can exceed 5.5V for longer than 1μsec. The power dissipated in the emitter junction during breakdown can destroy the junction. Current limiting provisions in accordance with the ABSOLUTE MAXIMUM RATINGS will ensure against catastrophic failure should breakdown occur.

INPUT CLAMP DIODES

MSI circuits contain input clamp diodes as shown in Figure 4. At the input, these diodes limit negative excursions which exceed -1V by providing a low impedance current source from GROUND through the forward biased diode clamp. The clamps are designed to minimize ringing which may be induced on interconnect wires in excess of six inches in length.

INPUT CLAMP DIODES

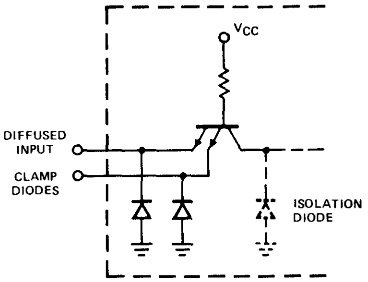


FIGURE 4

SIGNAL PROCESSING

The rise and fall times of all incoming data signals should be less than 200ns. The amplitude of incoming data signals should be 2.6V or greater. Figure 5 shows the transfer characteristic of the classic TTL gate. In the input threshold region, from point one to point two, the gate has approximately 25dB of gain. In this region, any discontinuity of the input waveform will be amplified more than 10 times at the output of the gate.

TTL TRANSFER CHARACTERISTIC

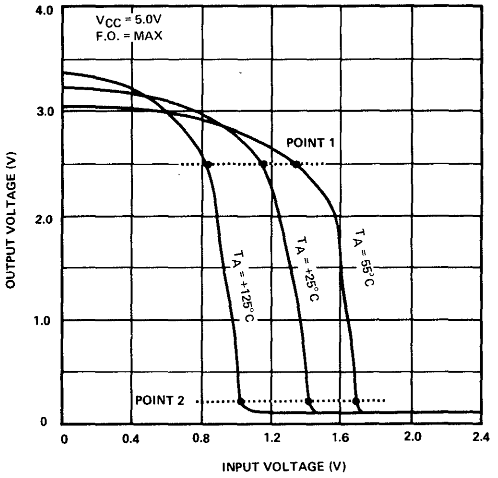


FIGURE 5

Should the input voltage remain in the threshold region (approximately 200mV wide) for more than 15ns, a typical TTL gate will oscillate as shown in Figure 6. The equivalent circuit in Figure 7 illustrates the potential oscillatory feed-back paths. The primary contributor to oscillation is the changing power supply voltage within the chip, caused by the current spiking which occurs during switching

DESIGN CONSIDERATIONS (Cont'd)

transitions. Since output voltage is directly proportional to V_{CC} and threshold voltage tends also to drop with lower supply voltage, the net effect is a positive feedback loop from output to input.

TYPICAL TTL GATE OSCILLATION

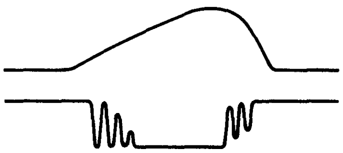


FIGURE 6

POTENTIAL OSCILLATORY FEEDBACK PATHS

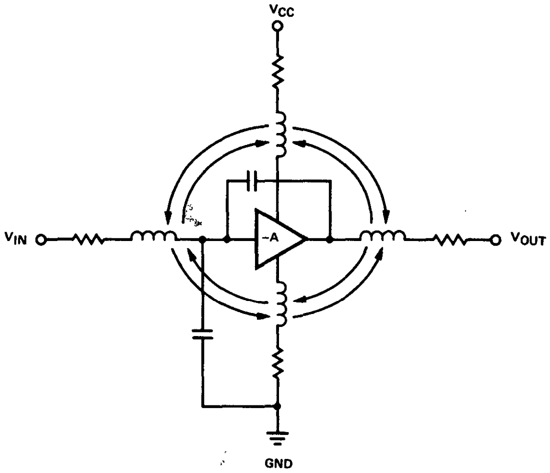
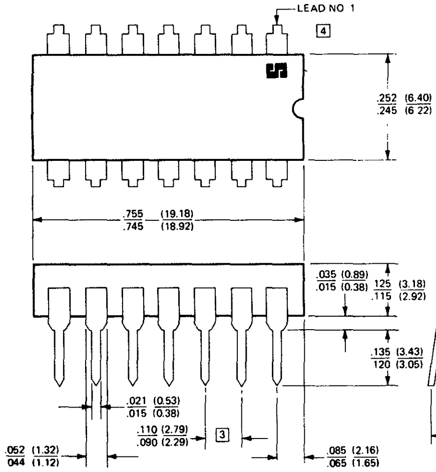


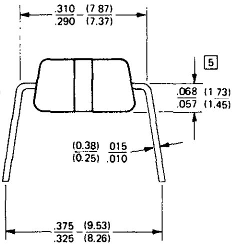
FIGURE 7

SECTION 4
PACKAGE TYPES

PACKAGE INFORMATION

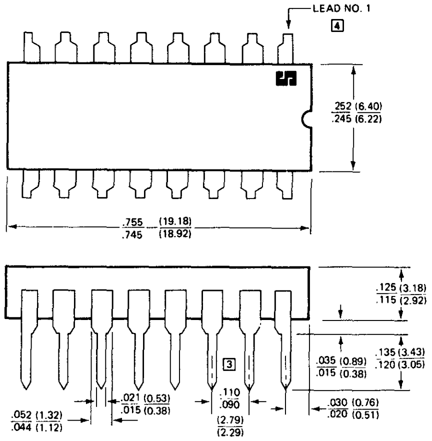
A PACKAGE
14 PIN DUAL IN-LINE, MOLDED

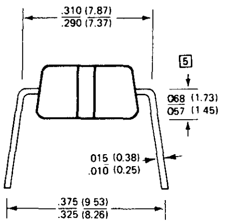




NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θ Ja = .16 C/mW, θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

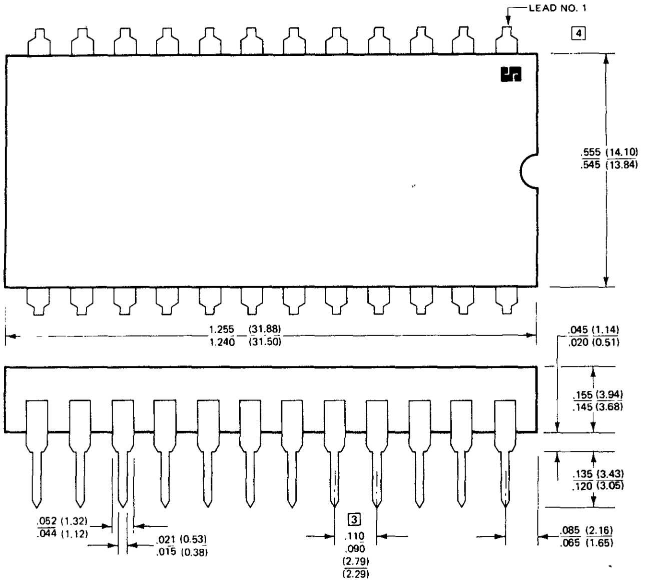
B PACKAGE
16 PIN DUAL IN-LINE, MOLDED



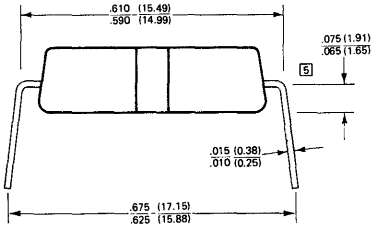


NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θ Ja = .16 C/mW, θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

N PACKAGE
24 PIN DUAL IN-LINE



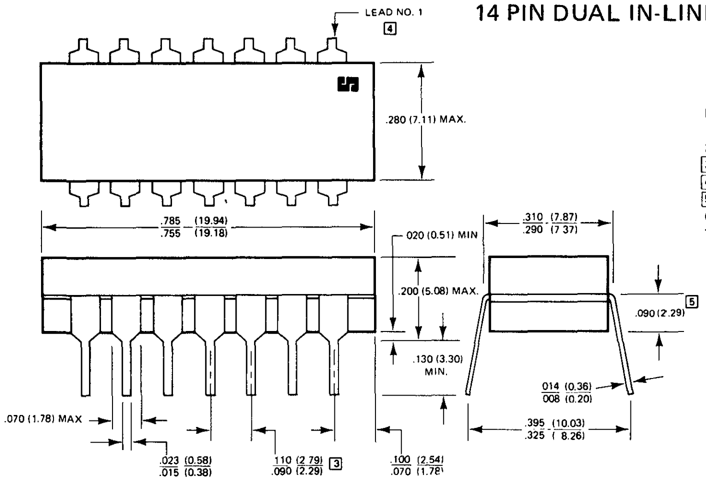
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θ Ja = .12 C/mW, θ Jc = .05 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)



PACKAGE INFORMATION (Cont'd)

F PACKAGE

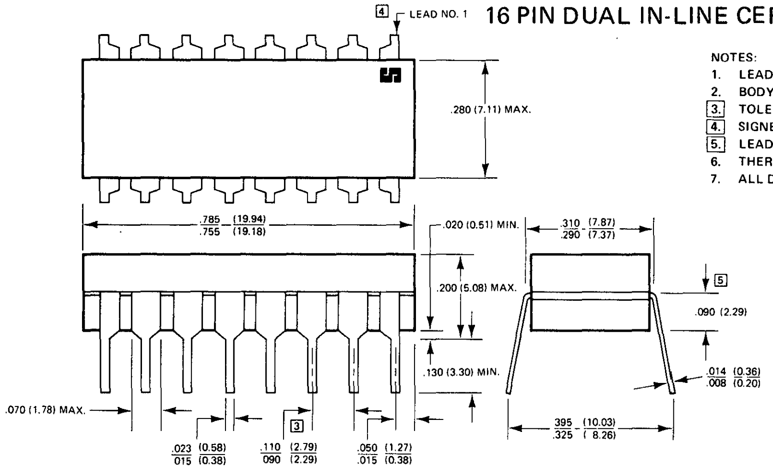
14 PIN DUAL IN-LINE CERDIP



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: Θ Ja = .065°C/mW, Θ Jc = .020°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

F PACKAGE

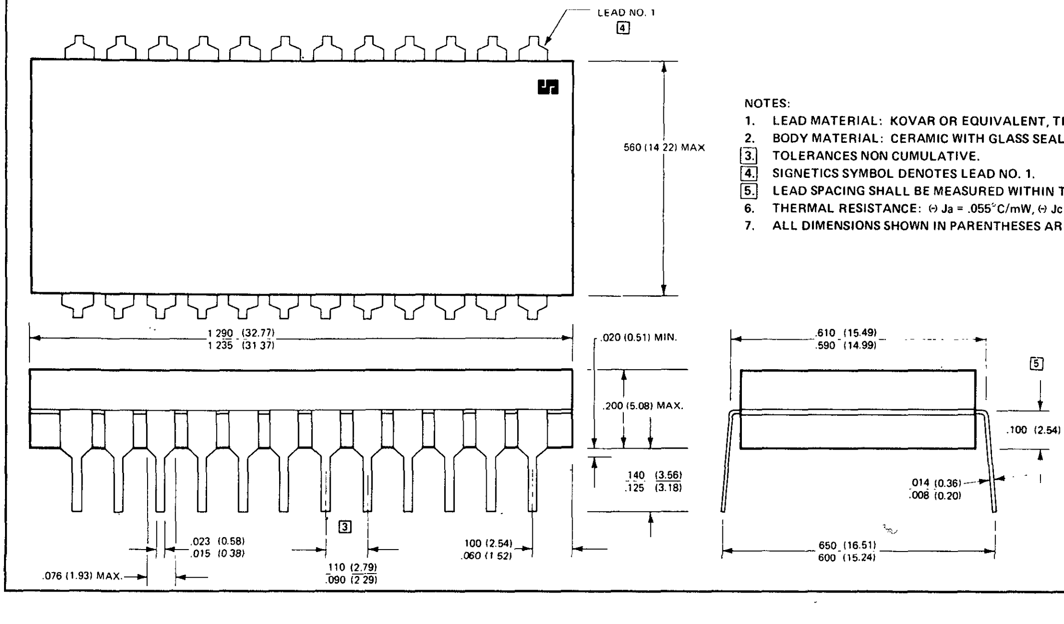
16 PIN DUAL IN-LINE CERDIP



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: Θ Ja = .090°C/mW, Θ Jc = .023°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

F PACKAGE

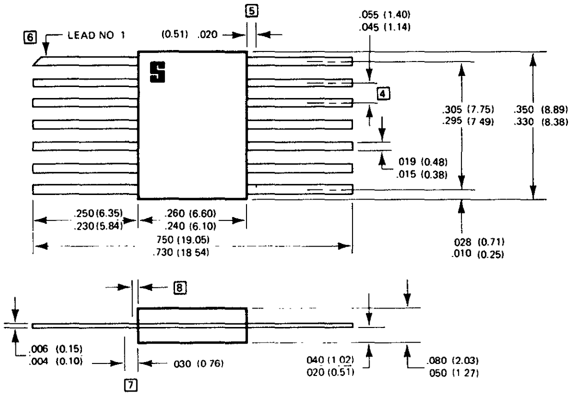
24 PIN DUAL IN-LINE CERDIP



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: Θ Ja = .055°C/mW, Θ Jc = .012°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

W PACKAGE

14 PIN FLAT, CERPAC

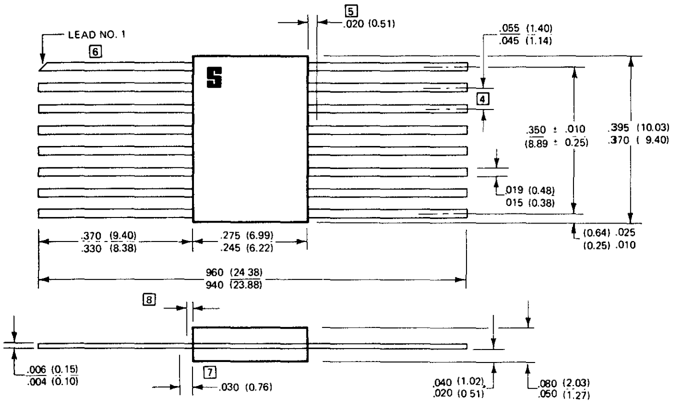


NOTES:

1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. MAXIMUM GLASS CLIMB .010.
9. THERMAL RESISTANCE: Θ Ja = .200°C/mW, Θ Jc = .085 C/mW.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

W PACKAGE

16 PIN FLAT, CERPAC

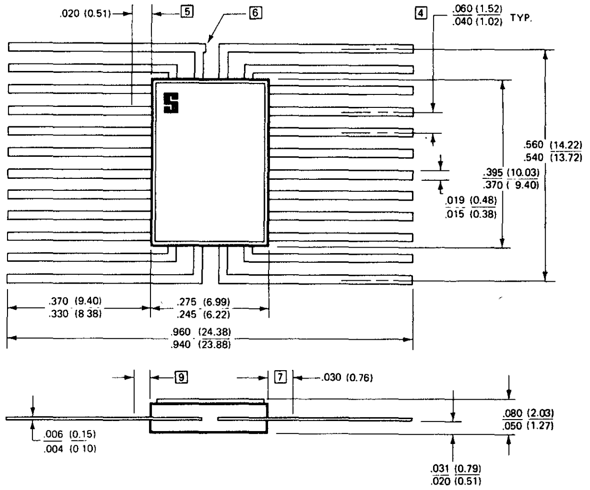


NOTES:

1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. MAXIMUM GLASS CLIMB .010.
9. THERMAL RESISTANCE: Θ Ja = .200 C/mW, Θ Jc = .085 C/mW.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

Q PACKAGE

24 PIN FLAT, CERAMIC



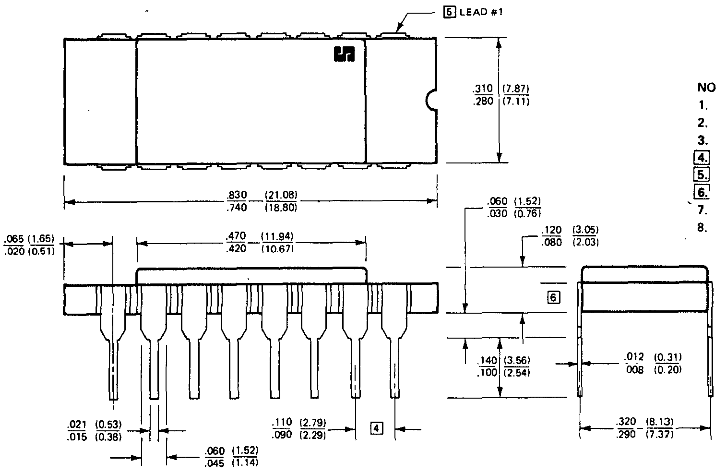
NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. THERMAL RESISTANCE: Θ Ja = .150 C/mW, Θ Jc = .050 C/mW.
9. MAXIMUM GLASS CLIMB, LID SKEW, OR FRIT SQUEEZE OUT IS .010.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

PACKAGE INFORMATION (Cont'd)

I PACKAGE

16 PIN DUAL IN-LINE CERAMIC

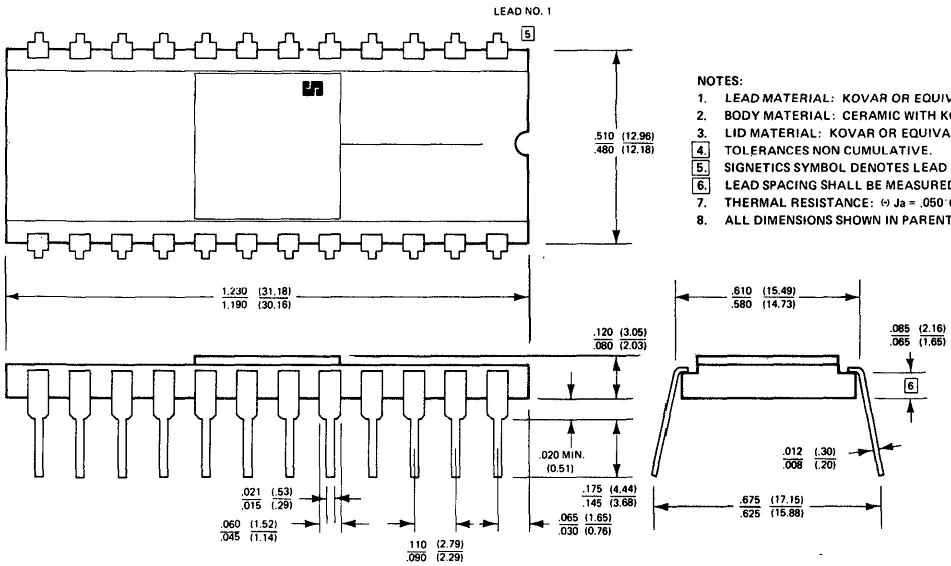


NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT. TOP RING GOLD PLATED.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .062 C/mW, Θ Jc = .018 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

Y PACKAGE

24 PIN DUAL IN-LINE, CERAMIC (.600 BEND—TOP BRAZED)



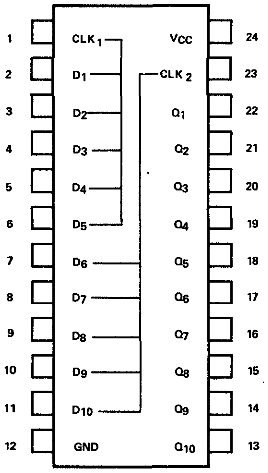
NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

SECTION 5
PIN CONFIGURATIONS

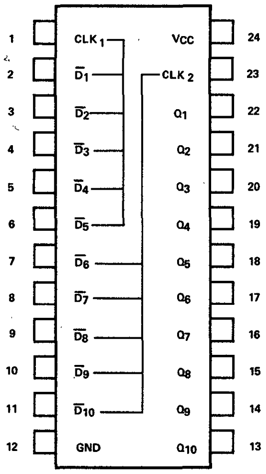
PIN CONFIGURATIONS

8200



Q,N,F PACKAGES

8201



Q,N,F PACKAGES

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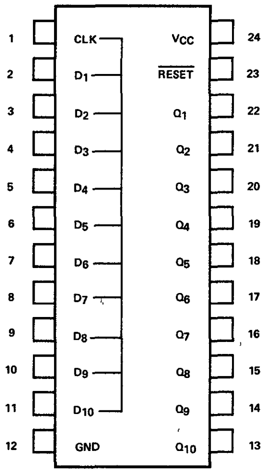
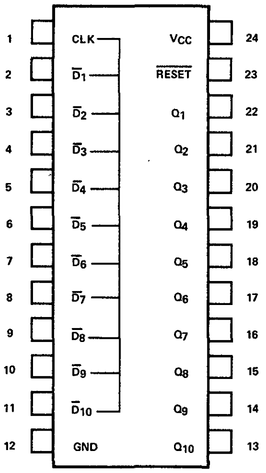


Q,N,F PACKAGES

8203



Q,N,F PACKAGES

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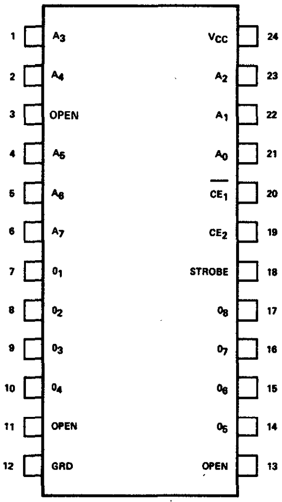

Y PACKAGE

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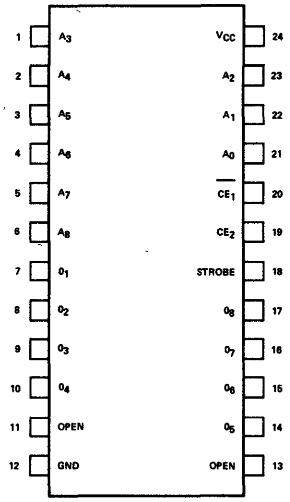
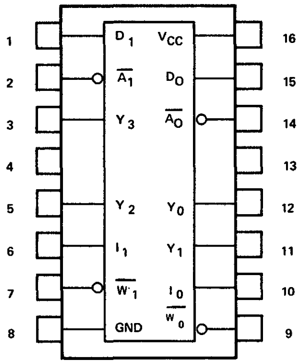


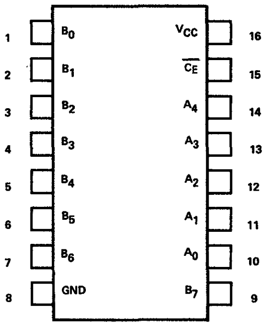
Y PACKAGE

8220



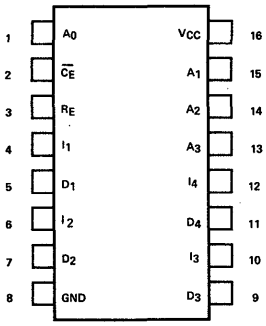
B PACKAGE

8223/24



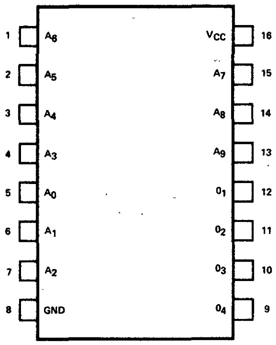
B,F,W PACKAGES

8225



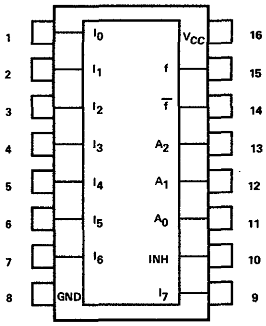
B,F, W PACKAGES

8228



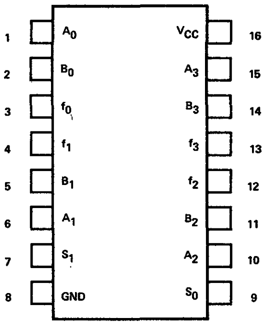
I PACKAGE

8230/31/32



B,F,W PACKAGES

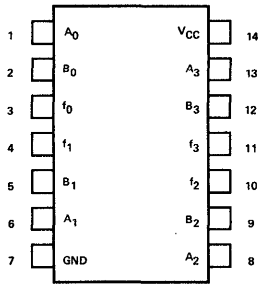
8233/34/35



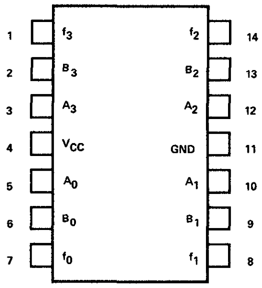
B,F,W PACKAGES

PIN CONFIGURATIONS (Cont'd)

8241/42

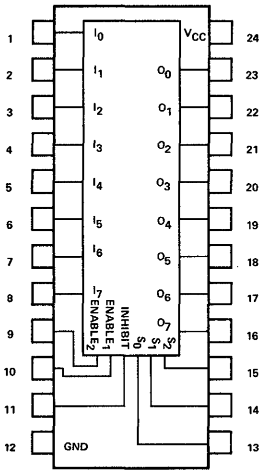


A,F PACKAGES



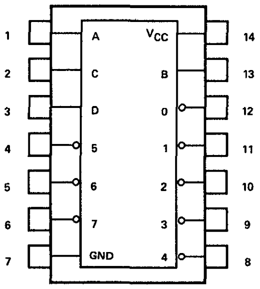
W PACKAGE

8243

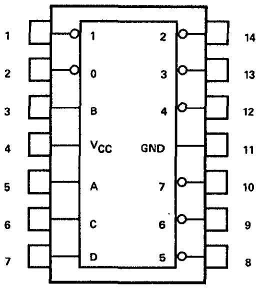


Q,N,Y PACKAGES

8250

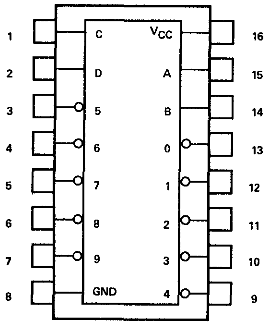


A,F PACKAGES



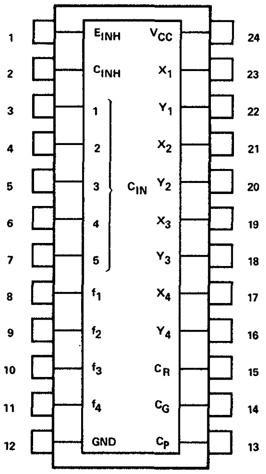
W PACKAGE

8251/52



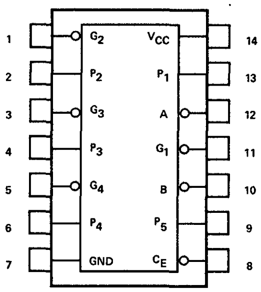
B,F,W PACKAGES

8260

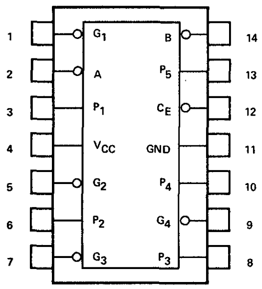


Q,N,YB PACKAGES

8261



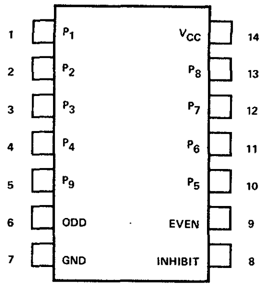
A,F PACKAGES



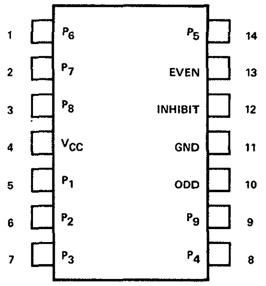
W PACKAGE

PIN CONFIGURATIONS (Cont'd)

8262

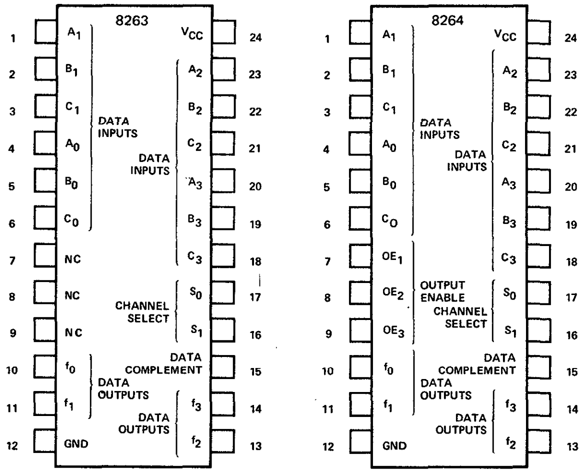


A,F PACKAGES



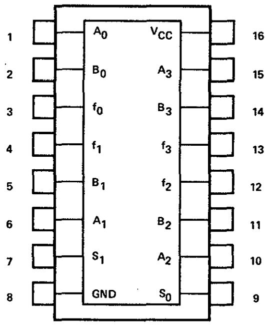
W PACKAGE

8263/64



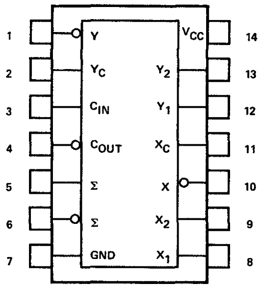
Q,N,Y PACKAGES

8266/67

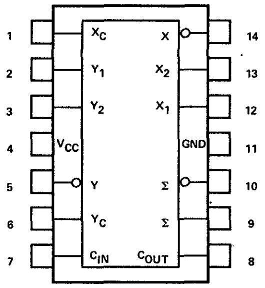


B,F,W PACKAGES

8268

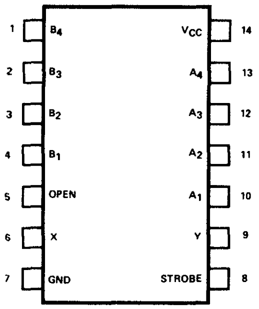


A,F PACKAGES

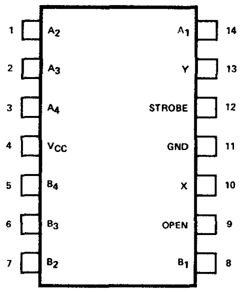


W PACKAGE

8269

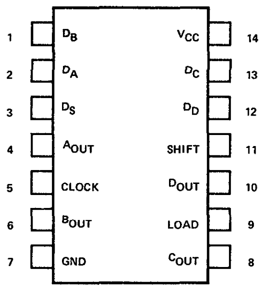


A,F PACKAGES

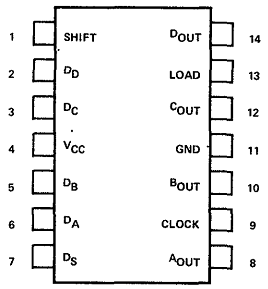


W PACKAGE

8270



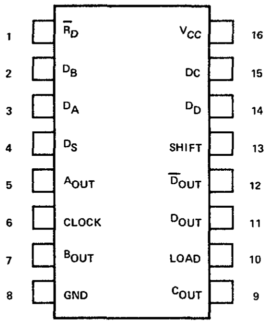
A,F PACKAGES



W PACKAGE

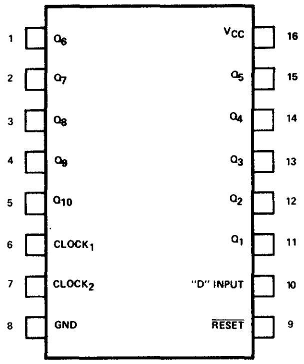
PIN CONFIGURATIONS (Cont'd)

8271



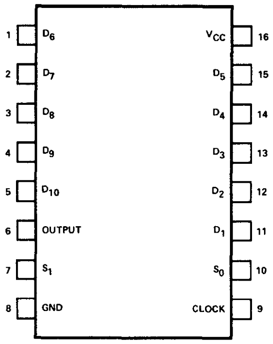
B,F,W PACKAGES

8273



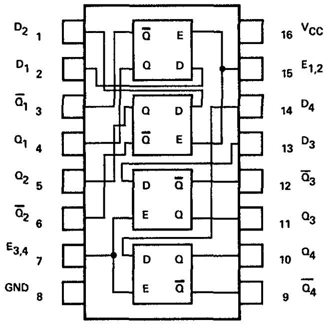
B,F,W PACKAGES

8274



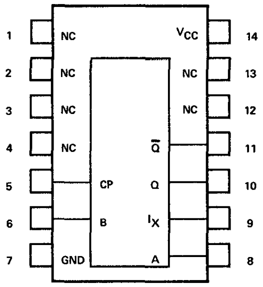
B,F,W PACKAGES

8275



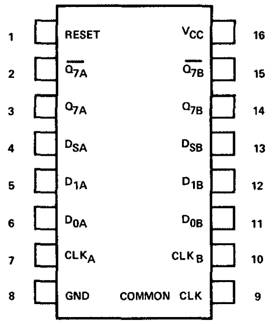
B,F,W PACKAGES

8276



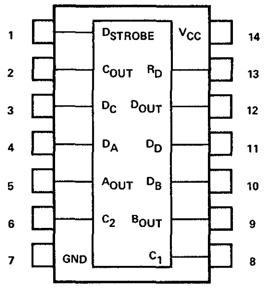
A,F PACKAGES

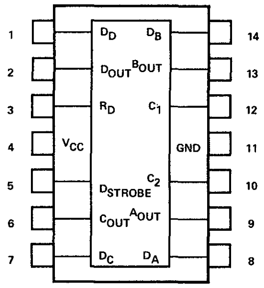
8277



B,F PACKAGES

8280/81

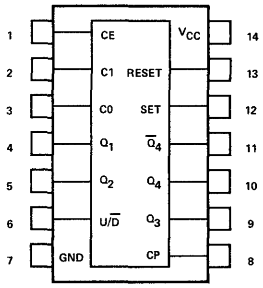


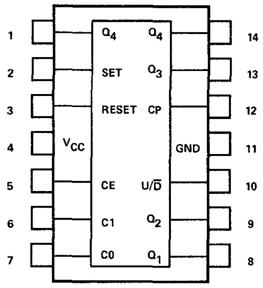


A,F PACKAGES

W PACKAGE

8284/85



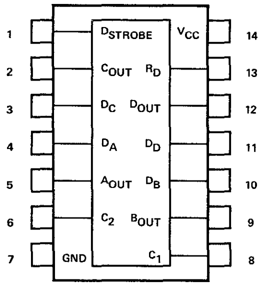


A,F PACKAGES

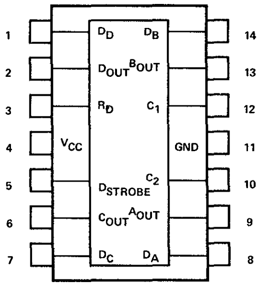
W PACKAGE

PIN CONFIGURATIONS (Cont'd)

8288

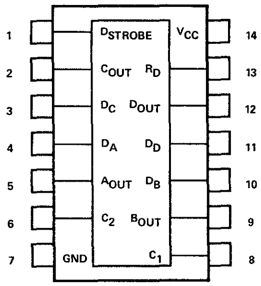


A,F PACKAGES

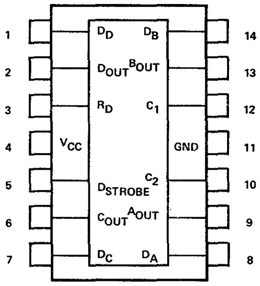


W PACKAGE

8290/91

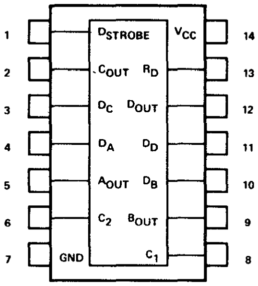


A,F PACKAGES

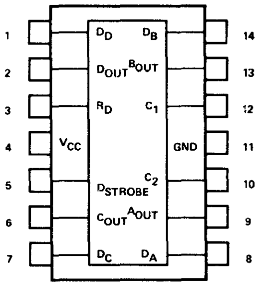


W PACKAGE

8292/93



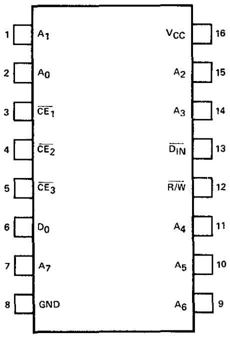
A,F PACKAGES



W PACKAGE

82S06/07

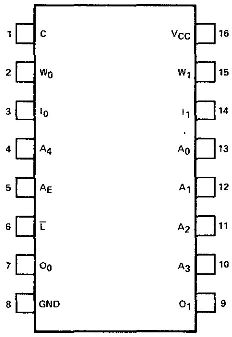
AVAILABLE SOON



DUAL IN-LINE PIN OUT

82S21

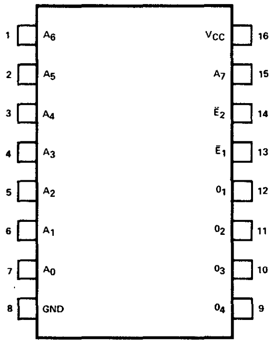
AVAILABLE SOON



DUAL IN-LINE PIN OUT

82S26/29

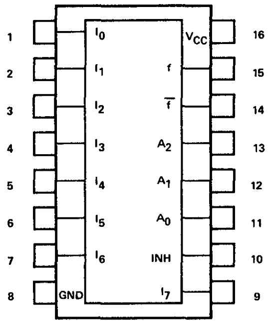
AVAILABLE SOON



DUAL IN-LINE PIN OUT

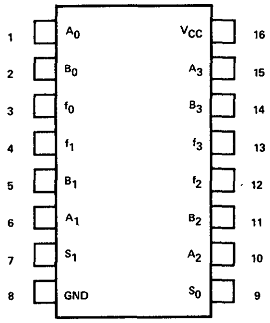
PIN CONFIGURATIONS (Cont'd)

82S30/31/32



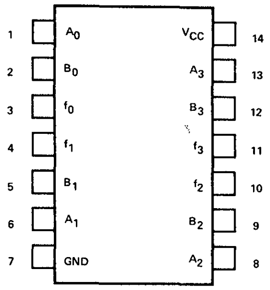
B,F PACKAGES

82S33/34



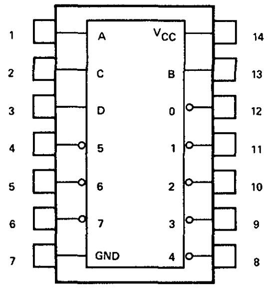
B,F PACKAGES

82S41/42

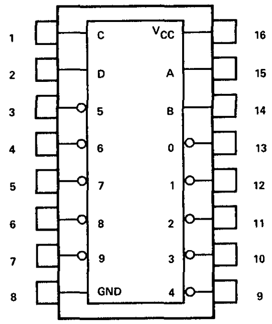


A,F PACKAGES

82S50/52

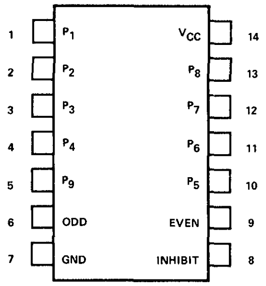


A,F PACKAGES

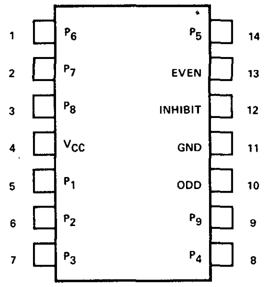


B,F PACKAGES

82S62

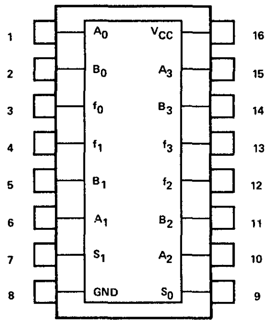


A,F PACKAGES



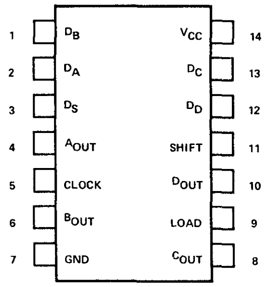
F,W PACKAGES

82S66/67

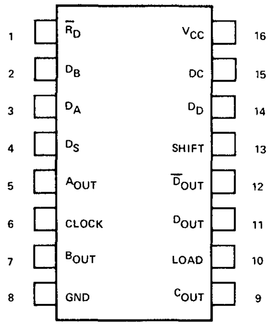


B,I PACKAGES

82S70/71



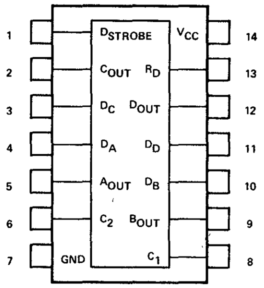
A,F PACKAGES



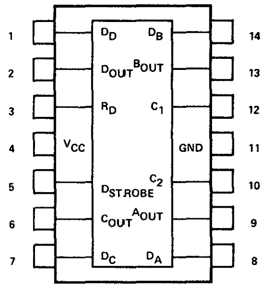
B,F PACKAGES

PIN CONFIGURATIONS (Cont'd)

82S90/91

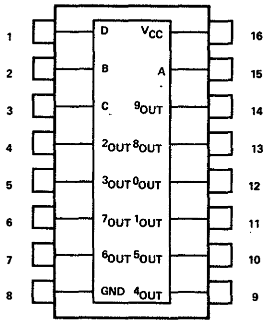


A,F PACKAGES



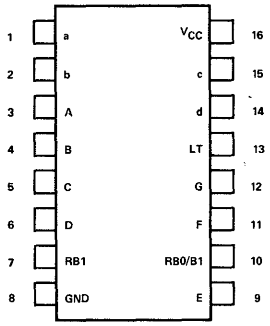
B,F PACKAGES

8T0l



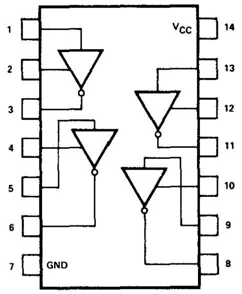
B,F PACKAGES

8T04/05/06

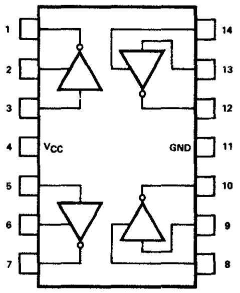


B,F,W PACKAGES

8T09

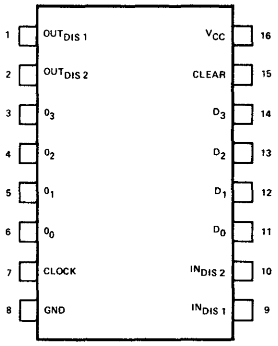


A,F PACKAGES



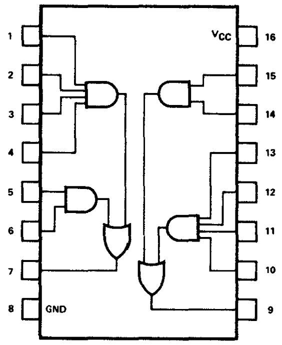
W PACKAGE

8T10



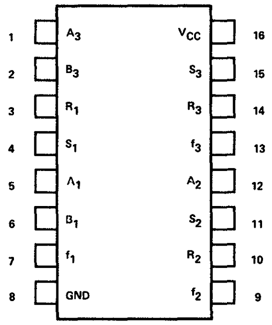
B,F,W PACKAGE

8T13



B,F,W PACKAGES

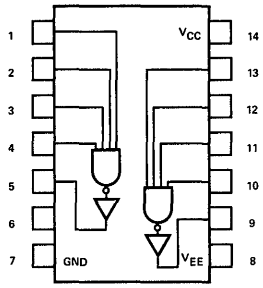
8T14



B,F,W PACKAGES

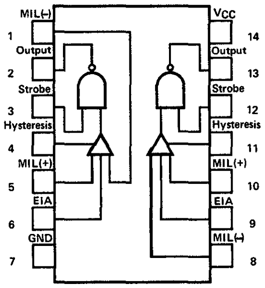
PIN CONFIGURATION (Cont'd)

8T15



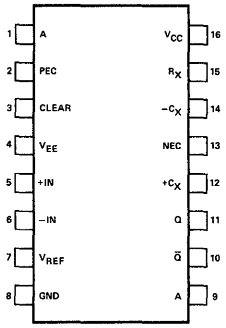
A,F PACKAGES

8T16



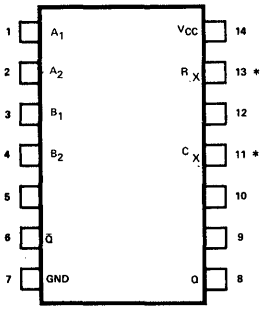
A,F PACKAGES

8T20



B,F PACKAGES

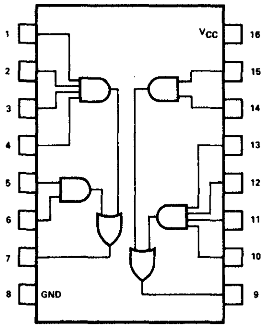
8T22



*Pins for External Timing Components

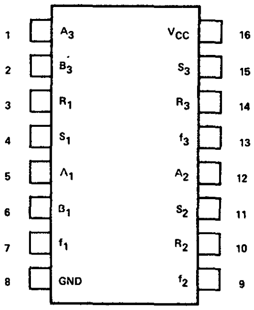
A,F PACKAGES

8T23



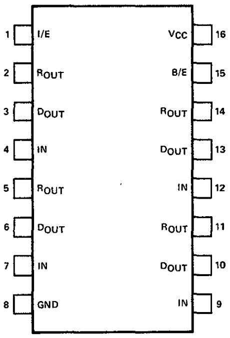
B,W PACKAGES

8T24



B,W PACKAGES

8T26



B,F PACKAGES

SECTION 6
ELECTRICAL CHARACTERISTICS

This section contains specific test limit and test condition information for use in device evaluation and incoming inspection for AC and DC parameters.

Product descriptions are also contained in this section to provide assistance in evaluating specific devices and total 8000 Series flexibility.

Unless otherwise specified, all devices are available in the "S" and "N" temperature ranges:

("S" = -55°C to +125°C, "N" = 0°C to +75°C).

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages in accordance with Table I. These ratings apply to both 82XX and 8TXX MSI devices unless otherwise specified.

TABLE I

Input Voltage	**+5.5V**
Output Voltage	**+7.0V**
V_{CC} (Note 2)	**+7.0V**
Storage Temperature Range	
A, B, N packages	**–65°C to +175°C**
F, I, Q, W packages	**–65°C to +200°C**

NOTES:

1. All devices must be derated at elevated temperatures based on maximum allowable junction temperature (see maximum storage temperature and the thermal resistance of the package.
2. Operating V_{CC} for the 8200 Series is specified at +5V±5%. None of the Signetics MSI elements will be damaged by supply voltages of 7 volts or less; however, in some of the more complex functions, power dissipation at such voltages could become excessive. We recommend, therefore, that such overvoltages be limited to a maximum of 1 second duration.

BUFFER REGISTERS

DIGITAL 8000 SERIES TTL/MSI

8200
8201
8202
8203

DESCRIPTION

The 8200/8201/8202/8203 MSI Buffer Registers are arrays of ten clocked "D" flip-flops especially suited for parallel in-parallel out register applications. They are also suitable for general purpose applications as parallel in-serial out, serial in-parallel out registers.

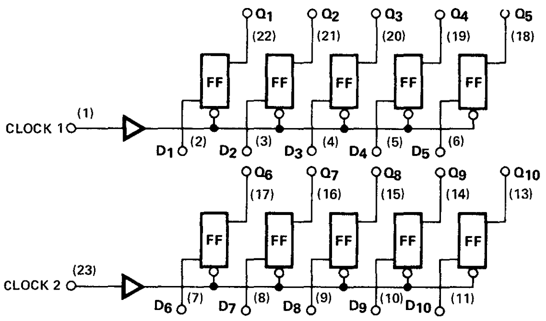
The flip-flops are arranged as dual 5 arrays, (8200 & 8201) and single 10 arrays with reset, (8202 & 8203). The true output of each bit is made available to the user.

The 8200 and 8202 feature true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock.

The 8201 and 8203 feature complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative going transition of the clock. This complementing input feature ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

LOGIC DIAGRAMS AND TRUTH TABLES

DUAL 5-BIT BUFFER REGISTER

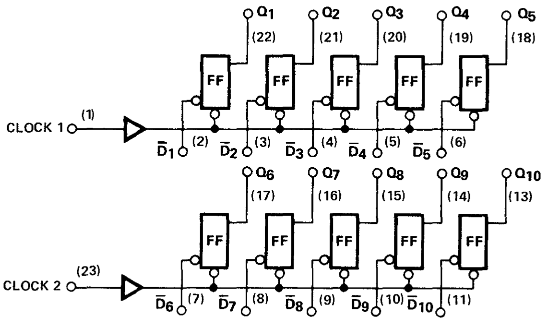


D_n	Q_{n+1}
1	1
0	0

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8200

DUAL 5-BIT BUFFER REGISTER—INVERTED INPUTS

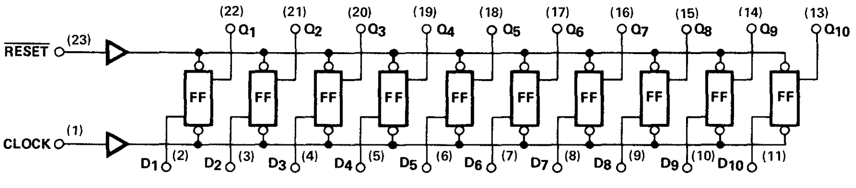


$\overline{D}_n$	Q_{n+1}
1	0
0	1

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8201

10-BIT BUFFER REGISTER



D_n	$\overline{\text{RESET}}$	Q_{n+1}
1	1	1
0	1	0

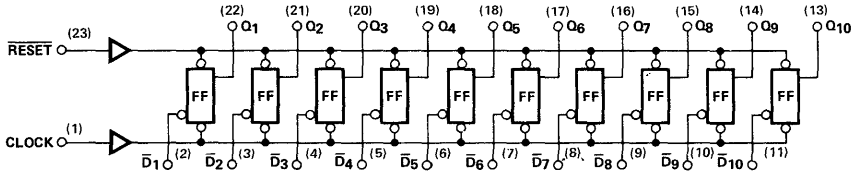
$\overline{\text{RESET}} = 0 \Rightarrow Q = 0$
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8202

LOGIC DIAGRAMS AND TRUTH TABLES (Cont'd)

10-BIT BUFFER REGISTER–INVERTED INPUTS



$\overline{D}_n$	$\overline{\text{RESET}}$	Q_{n+1}
0	1	1
1	1	0

$\overline{\text{RESET}}$ = 0 ⇒ Q = 0
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8203

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n 8200 8202	$\overline{D}_n$ 8201 8203	CLOCK	$\overline{\text{RESET}}$ 8202 8203	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	0.8V	Pulse		800µA	6
"0" Output Voltage			0.4	V	0.8V	2.0V	Pulse		9.6mA	7
"0" Input Current										
D_n(8200, 8202)	-0.1		-1.6	mA	0.4V					
$\overline{D}_n$(8201, 8203)	-0.1		-1.6	mA		0.4V				
$\overline{\text{Clock}}$	-0.1		-1.6	mA			0.4V			
$\overline{\text{Reset}}$ (8202, 8203)	-0.1		-1.6	mA				0.4V		
"1" Input Current										
D_n (8200, 8202)			40	µA	4.5V					
$\overline{D}_n$ (8201, 8203)			40	µA		4.5V				
Clock			40	µA			4.5V			
Reset (8202, 8203)			40	µA				4.5V		
Input Voltage Rating										
(All inputs)	5.5			V	10mA	10mA	10mA	10mA		
Power/Current Consumption		409/77.7	580/110	mW/mA	0V	0V	0V			11,13

T_A = 25°C and V_{CC} = 5.0V

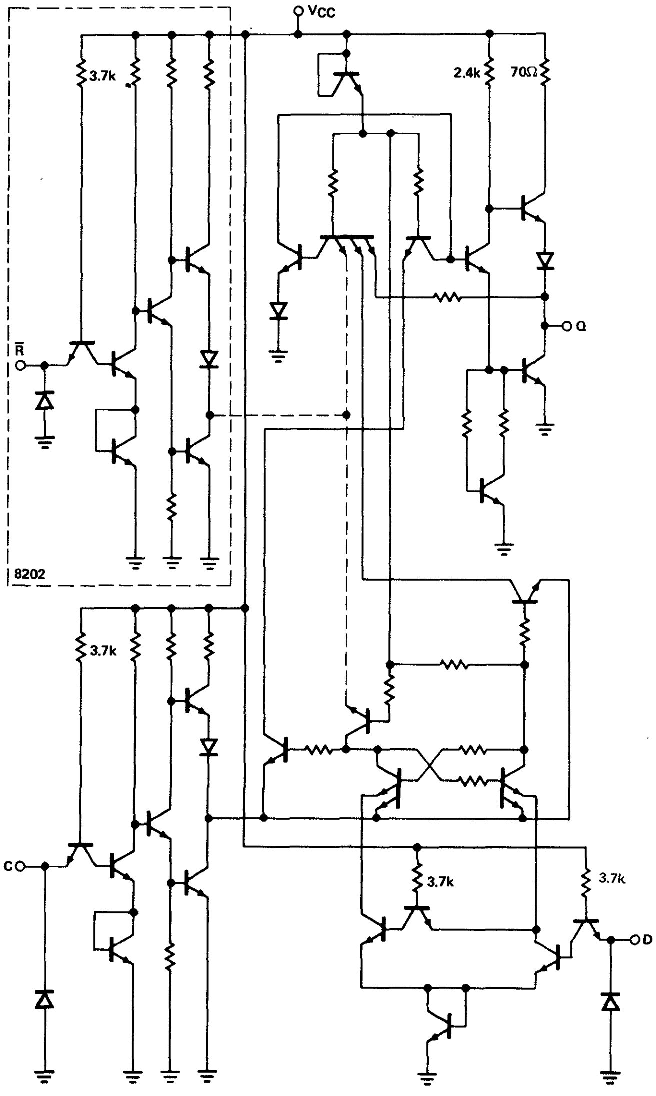
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Propagation Delay						
t_{on} Clock to Q		30	45	ns		8
t_{off} Clock to Q		25	40	ns		8
t_{on} Reset to Q		30	45	ns		8
Set Up Time		6	15	ns		10
Hold Time		0	5	ns		12
Minimum Clock Width		12	17	ns		
Transfer Rate	15	35		MHz		8
Output Short Circuit Current	-20		-70	mA		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to V_{CC}.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Set Up Time defined as data presence before clock.
11. Outputs are in the low state for this test.
12. Hold time defined as data presence after clock.
13. V_{CC} = 5.25 volts.

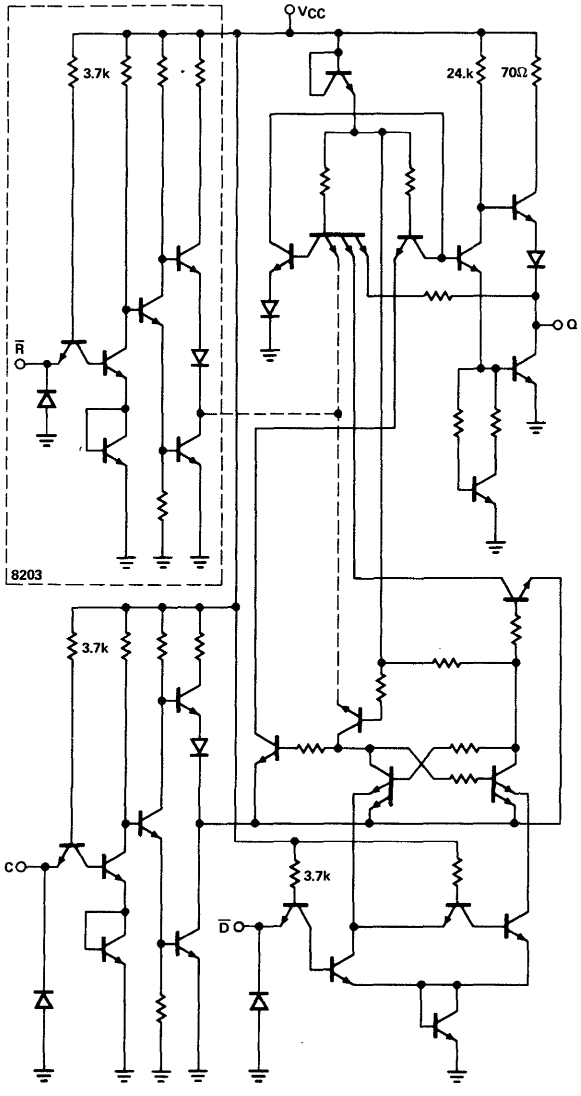
SCHEMATIC DIAGRAMS

DUAL 5-BIT BUFFER REGISTER 8200
SINGLE 10-BIT BUFFER REGISTER 8202



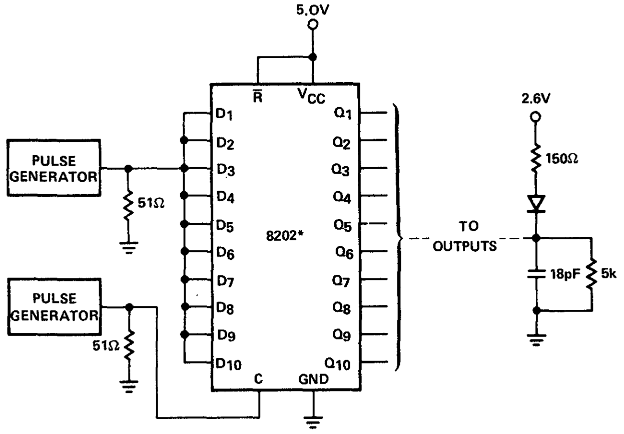
DUAL 5-BIT BUFFER REGISTER
–INVERTED INPUTS 8201

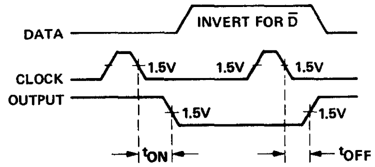
SINGLE 10-BIT BUFFER REGISTER
–INVERTED INPUTS 8203



AC TEST FIGURES AND WAVEFORMS

t_{pd} FROM CLOCK TO Q

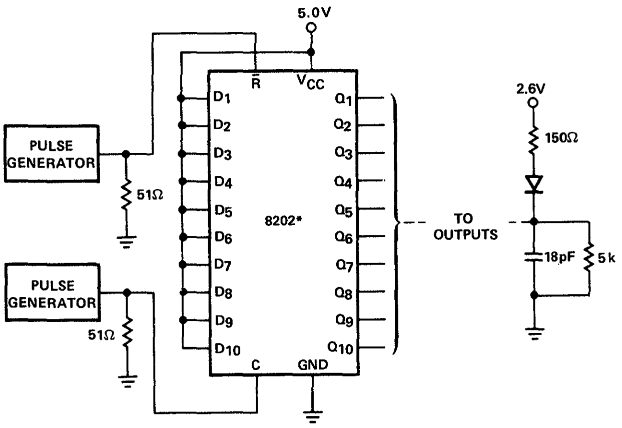


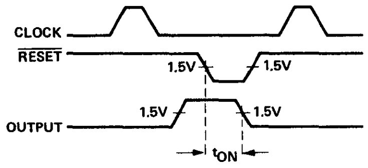


INPUT PULSE:
Data = P.R.R. = 7.5 MHz
Clock = P.R.R. = 15 MHz
PW = 17 ns (at 50% point)
$t_r = t_f = 5$ ns Max.
Amplitude = 2.6V.

*Refer to the Pin-Outs for the 8200/01/03 AC Testing.

t_{on} FROM $\overline{\text{RESET}}$ TO Q



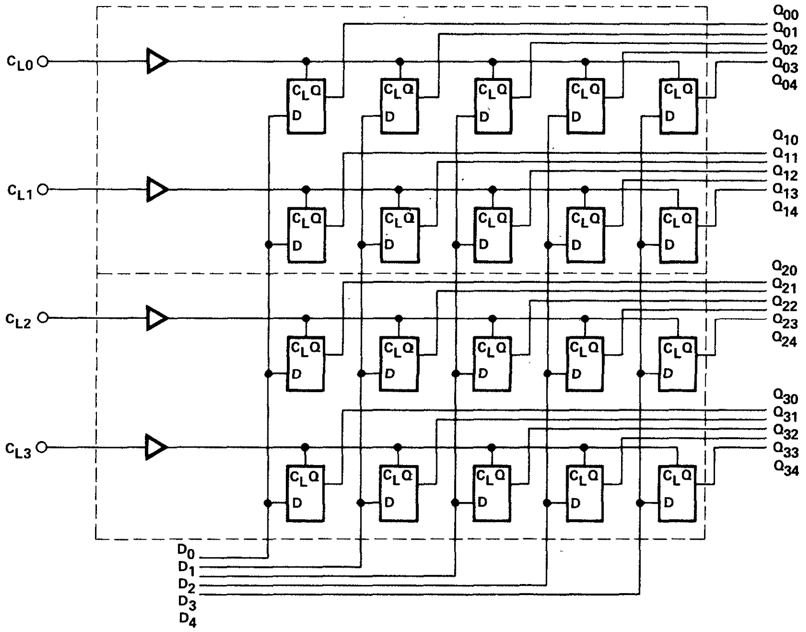


INPUT PULSE:
Amplitude = 2.6V
Clock: P.R.R. = 5 MHz
$\overline{\text{Reset}}$: P.R.R. = 5 MHz
PW = 30 ns (at 50% point)
$t_r = t_f = 5$ ns

*Refer to the Pin-Outs for the 8200/01/02/03 AC Testing.

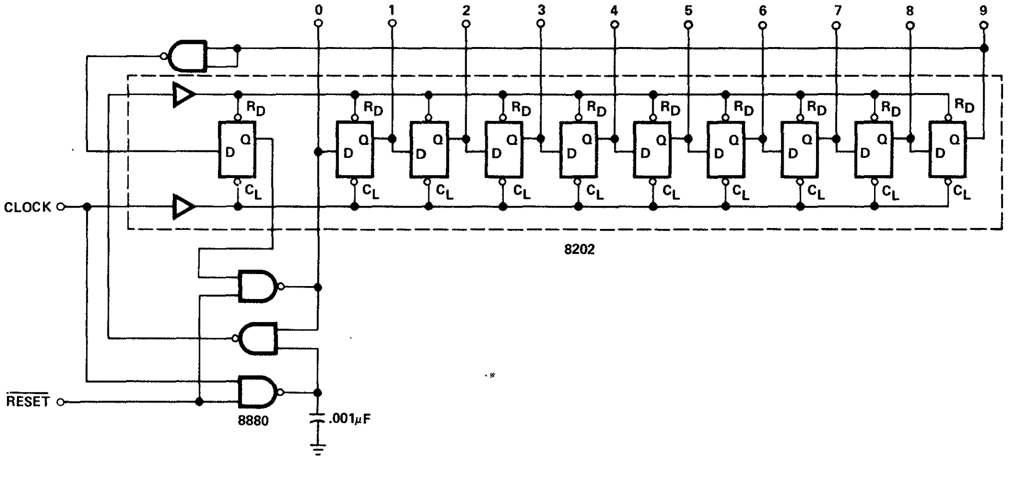
TYPICAL APPLICATIONS

20 BIT (4 WORDS X 5 BITS EACH) MEMORY CELL



Total Package Count = 2-8200's

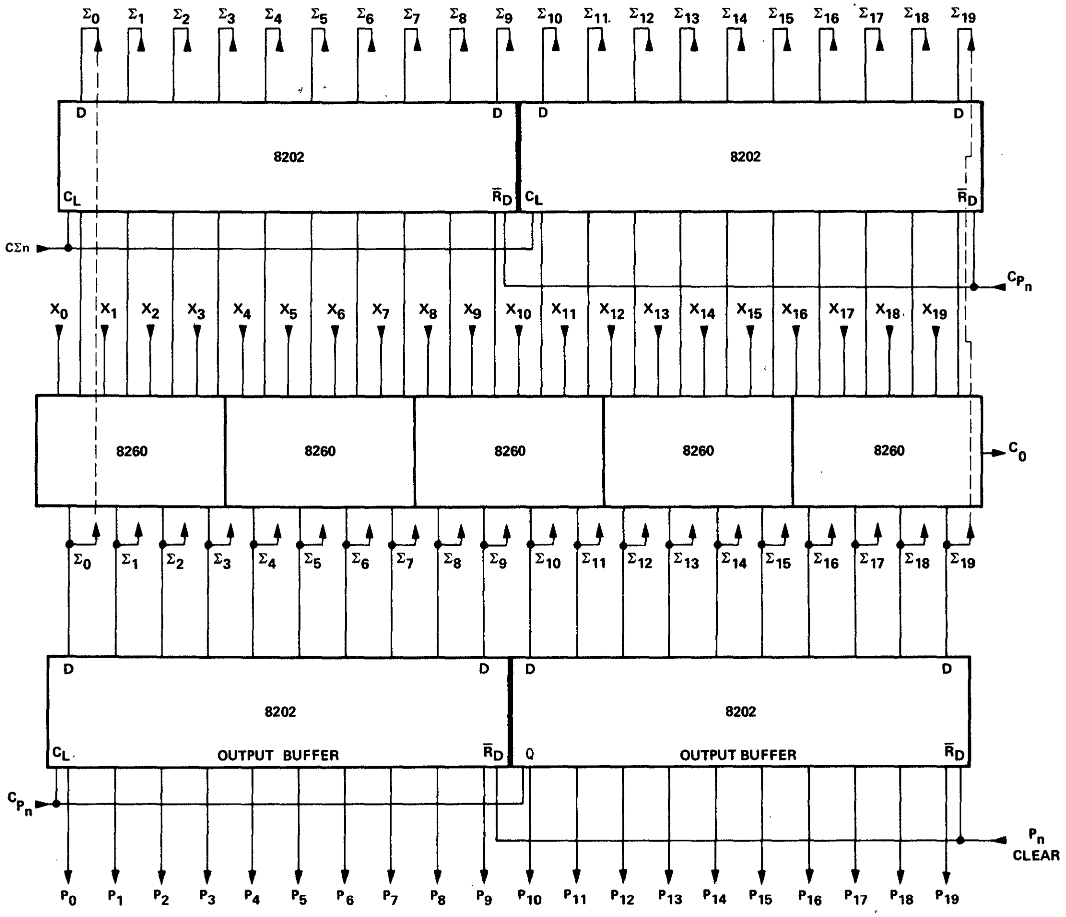
ONE OUT OF TEN – COUNTER/DISPLAY (SELF-CORRECTING)



Total Package Count = 1-8202; 1-8880

TYPICAL APPLICATIONS (Cont'd)

MULTIPLICATION AT 10MHz OF A 20-BIT BINARY WORD



$P_n = (X_n)M$ WHERE $X_n \equiv$ MULTIPLICAND
M ≡ MULTIPLIER
TOTAL PACKAGE COUNT = 9 PACKAGES (4-8202'S AND 5-8260'S)

8-INPUT DIGITAL MULTIPLEXER

8230
8231
8232

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 8230 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the $\overline{f}$ output. With the INHIBIT input high, the f output is unconditionally low and the $\overline{f}$ output is unconditionally high. The 8230 is a functional and pin-for-pin replacement for the 9312.

The 8231 is a variation of the 8230 that provides open collector output $\overline{f}$ for expansion of input terms. The 8232 is similar to the 8230 except in the effect of the INHIBIT input on the $\overline{f}$ output. With the INHIBIT low, the selected input appears at the f output and, in complement, on the $\overline{f}$ output. With the INHIBIT input high, both the f and the $\overline{f}$ output are unconditionally low.

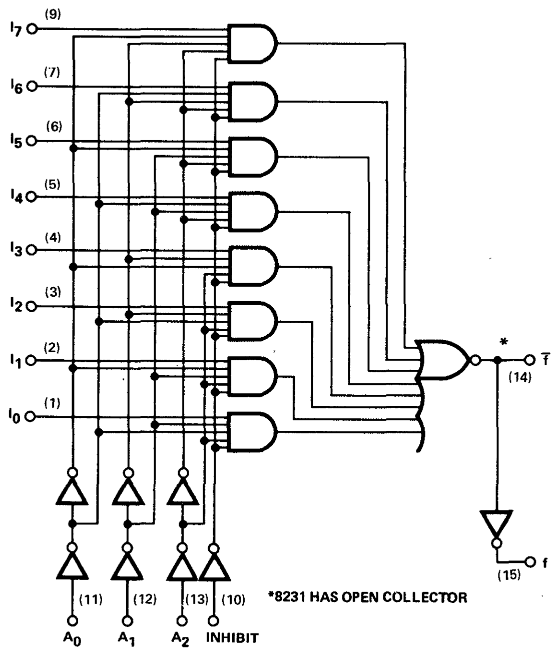
TRUTH TABLE

ADDRESS			DATA INPUTS									OUTPUT		
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	f	8230 8231 $\overline{f}$	8232 $\overline{f}$
0	0	0	x	x	x	x	x	x	x	1	0	1	0	0
0	0	1	x	x	x	x	x	x	1	x	0	1	0	0
0	1	0	x	x	x	x	x	1	x	x	0	1	0	0
0	1	1	x	x	x	x	1	x	x	x	0	1	0	0
1	0	0	x	x	x	1	x	x	x	x	0	1	0	0
1	0	1	x	x	1	x	x	x	x	x	0	1	0	0
1	1	0	x	1	x	x	x	x	x	x	0	1	0	0
1	1	1	1	x	x	x	x	x	x	x	0	1	0	0
0	0	0	x	x	x	x	x	x	x	0	0	0	1	1
0	0	1	x	x	x	x	x	x	0	x	0	0	1	1
0	1	0	x	x	x	x	x	0	x	x	0	0	1	1
0	1	1	x	x	x	x	0	x	x	x	0	0	1	1
1	0	0	x	x	x	0	x	x	x	x	0	0	1	1
1	0	1	x	x	0	x	x	x	x	x	0	0	1	1
1	1	0	x	0	x	x	x	x	x	x	0	0	1	1
1	1	1	0	x	x	x	x	x	x	x	0	0	1	1
x	x	x	x	x	x	x	x	x	x	x	1	0	1	0

x = don't care

LOGIC DIAGRAMS

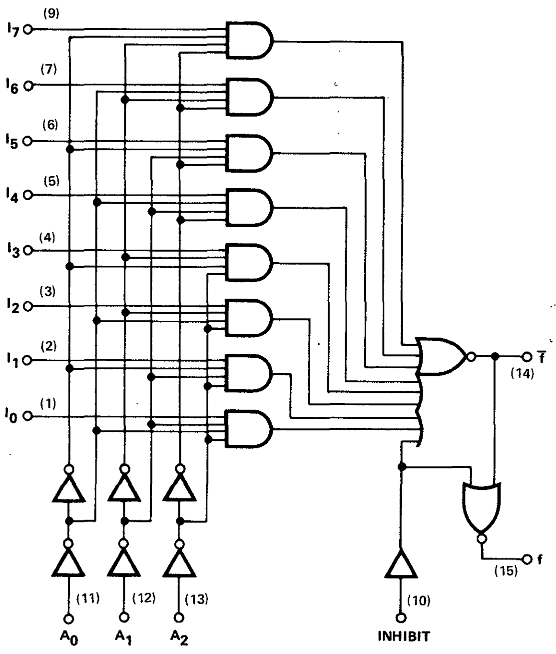
8230 AND 8231



*8231 HAS OPEN COLLECTOR

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

8232



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	A_1	A_2	A_3	INH	DATA INPUT In	OUTPUTS	
"1" Output Voltage, Output f	2.6	3.5		V	*	*	*	0.8V	2.0V	-800µA	6, 11
Output $\overline{f}$ (8230, 8232)	2.6	3.5		V	*	*	*	2.0V	*	-800µA	6, 11
"1" Output Leakage Current, Output $\overline{f}$ (8231)			150	µA	0.8V	2.0V	2.0V	2.0V	0.6V		14
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V	0.8V	0.8V	16mA	7, 11
"1" Input Current											
Inputs An, I_n			40	µA	4.5V	4.5V	4.5V		4.5V		
Input INH, 8230 & 8231			80	µA				4.5V			
Input INH, 8232			80	µA				4.5V			
"0" Input Current											
A_n, I_n, INH (8230 & 8231)	-0.1		-1.6	mA	0.4V	0.4V	0.4V		0.4V		
INH, (8232)	-0.1		-3.2	mA				0.4V			

T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	A	A	A	INH	DATA INPUT In	OUTPUTS f $\overline{f}$	
Propagation Delay											
A_n to $\overline{f}$ (8230, 8232)		19	30	ns							8
A_n to $\overline{f}$ (8231)		17	30	ns							8
I_n to $\overline{f}$ (8230, 8232)		11	20	ns							8
$\overline{f}$ to f		10	15	ns							8
I_n to $\overline{f}$ (8231)		13	24	ns							8
INH to $\overline{f}$ (8230, 8231)		18	30	ns							8
INH to f or $\overline{f}$ (8232)		11	20	ns							8
Power Consumption/Supply Current											
8230, 8231			250/ 47.7	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		13
8232			262/ 50.0	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		13
Output Short Circuit Current											
Output f	-20		-70	mA	0V	0V	0V	0V	4.5V	0V	
Output $\overline{f}$ (8230, 8232)	-20		-70	mA	0V	0V	0V	0V	0V	0V	
Input Latch Voltage	5.5			V	10mA	10mA	10mA	10mA	10mA		12

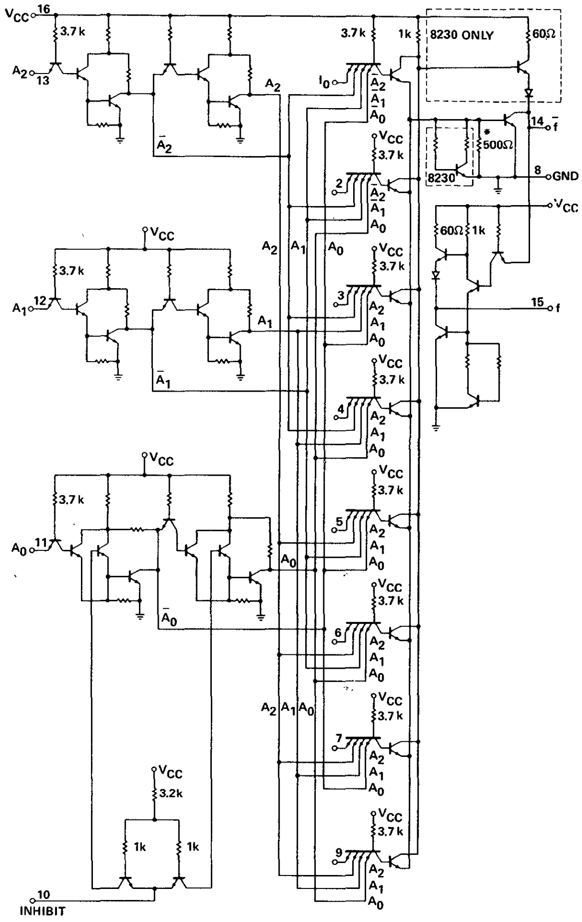
*See Truth Table for Logical Conditions

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. One AC fan-out is defined as 50pF.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
12. This test guarantees operation free of input latch-up over the specific operating power supply voltage range.
13. All I_n data inputs are at 0V. V_{CC} = 5.25V.
14. Connect an external 1k resistor from V_{CC} to the output terminal for this test.

SCHEMATIC DIAGRAMS

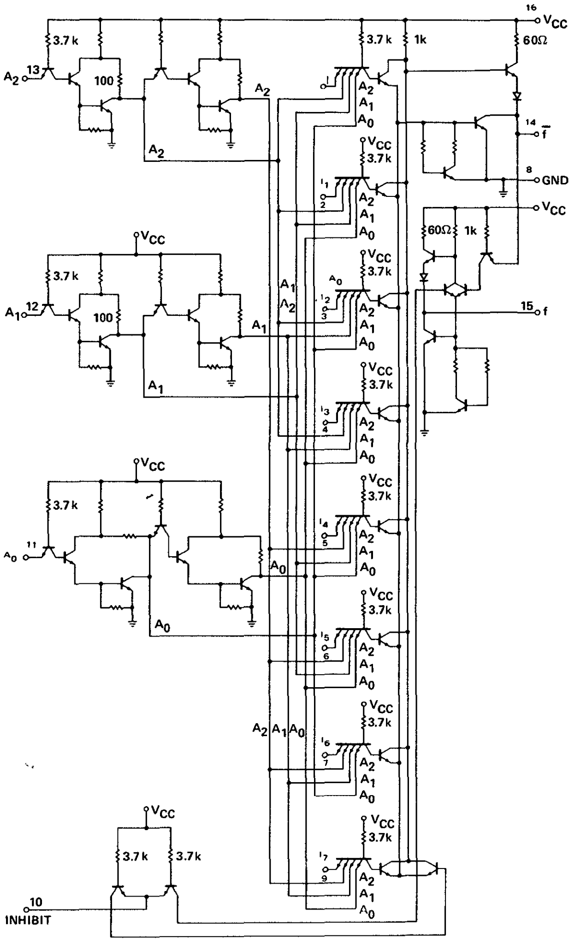
8230 AND 8231



*500Ω Resistor on 8231 only.

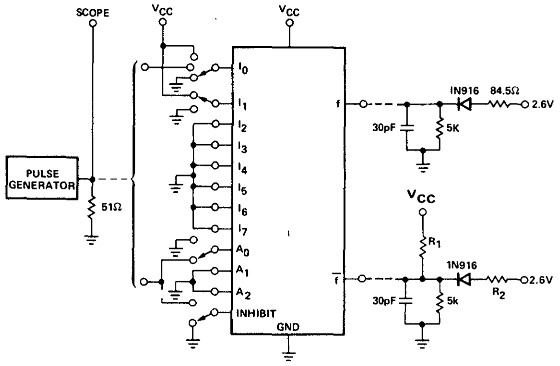
Note: All inputs have diode clamping. All outputs have isolation diodes.

8232



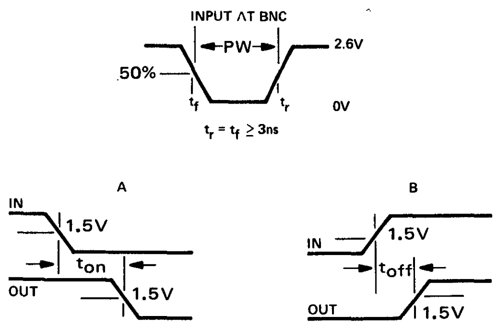
Note: All inputs have diode clamping. All outputs have isolation diodes.

AC TEST FIGURE AND WAVEFORMS

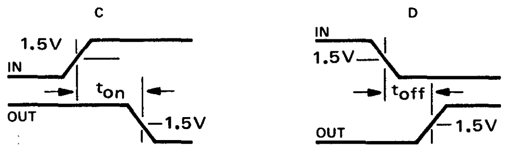


	8320/32	8231
R_1	∞	360Ω
R_2	84.5Ω	440Ω

NON-INVERTING PATHS



INVERTING PATHS



NOTES:
1. 5K, 30pF load includes test jigs and scope impedance.
2. Scope terminals to be ≤ 1½" from package pins.
3. See truth table for logical conditions.

AC TEST CONDITIONS

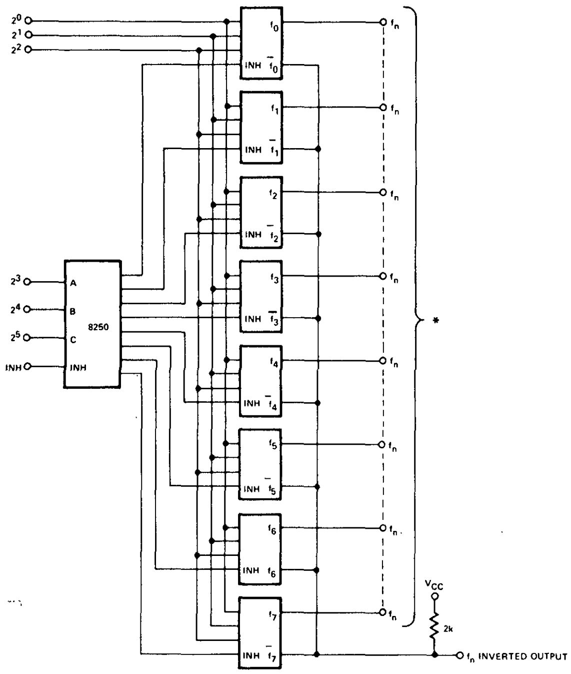
STEP NO.	TYPE/S	DELAY FROM-TO	INPUTS				WAVE-FORM TYPE
			I_0	I_1	A_0	INH	
1	ALL	A_0 to $\bar{f}$	0 V	V_{CC}	P.G.	0 V	C, D
2	ALL	I_0 to $\bar{f}$	P. G.	0 V	0 V	0 V	C, D
3	ALL	$\bar{f}$ to f*	P. G.	0 V	0 V	0 V	C, D
4	8230 8231	INH to $\bar{f}$	V_{CC}	0 V	0 V	P. G.	A, B
5	8232	INH to $\bar{f}$	0 V	0 V	0 V	P. G.	C, D
6	8232	INH to f	V_{CC}	0 V	0 V	P. G.	C, D

NOTE: 1. P. G. = Pulse Generator

*Both f and $\bar{f}$ are simultaneously loaded.

TYPICAL APPLICATIONS

EXPANSION OF 8231 TO MULTIPLEXER 64 LINES



$*f_n = f_0 + f_1 + f_2 ..... f_7$

True Output

All Outputs may be tied together
to drive 8x16mA (eight 1.6mA F.O.)
or each Output may drive separately
ten 1.6mA F.O.

Note:

Each 8231 has 8 data inputs which are not shown.

2-INPUT 4-BIT DIGITAL MULTIPLEXER

8233
8234
8235

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

These devices are 2-input, 4-Bit Digital Multiplexers designed for general purpose data-selection applications.

The 8233 features *non-inverting* data paths; and, the 8234 features *inverting* data paths.

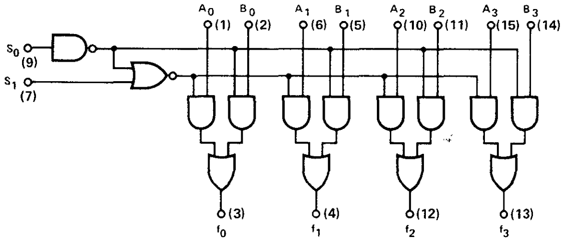
The 8235 is designed for input to adders, registers and general paralleled data handling due to its capability to perform CONDITIONAL COMPLEMENTING (TRUE/COMPLEMENT). When the two inputs for each bit position (Ai, Bi) are connected together, the f output will provide either the *True* or *Complement* of the input data. This capability is especially useful for transferring data into parallel adders where both true data for adding or multiplying and also complemented data for subtracting or dividing are needed.

The 8234 and 8235 designs have open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty 8234/8235s in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

LOGIC DIAGRAM AND TRUTH TABLES

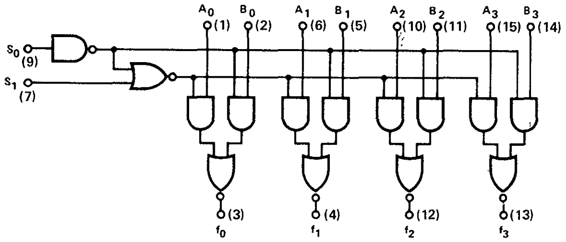
8233



S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

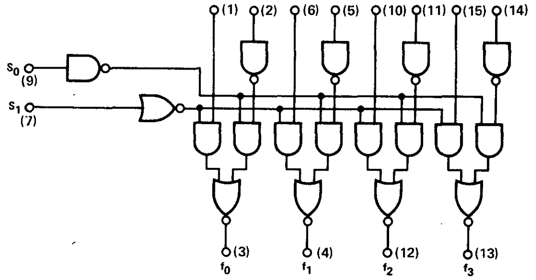
8234



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

8235



S_0	S_1	f_n
0	0	$\overline{A_n}B_n$
0	1	B_n
1	0	$\overline{A_n}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					INPUTS					
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1		
"1" Output Voltage (8233)	2.6	3.5		V	2.0V	2.0V	0.8V	0.8V	-800μA	6
"0" Output Voltage (8233)			0.4	V	0.8V	2.0V	2.0V	0.8V	16mA	7
"0" Output Voltage (8234)			0.4	V	0V	2.0V	0.8V	0.8V	16mA	7
"0" Output Voltage (8235)			0.4	V	2.0V	2.0V	2.0V	0.8V	16mA	7
"1" Output Leakage Current										
(8234)			100	μA	2.0V	2.0V	2.0V	2.0V	5.0V	13
"1" Output Leakage Current										
(8235)			100	μA	2.0V	2.0V	2.0V	2.0V	5.0V	13
"0" Input Current										
A_n	-0.1		-1.6	mA	0.4V	4.5V		0V		
B_n	-0.1		-1.6	mA	4.5V	0.4V	0V	0V		
S_0	-0.1		-1.6	mA			0.4V			
S_1	-0.1		-1.6	mA				0.4V		
"1" Input Current										
A_n			40	μA	4.5V	0V				
B_n			40	μA	0V	4.5V				
S_0			40	μA			4.5V			
S_1			40	μA				4.5V		
Input Latch Voltage										
A_n	5.5			V	10mA	0V				11
B_n	5.5			V	0V	10mA				11
S_0	5.5			V			10mA			11
S_1	5.5			V				10mA		11
Output Short Circuit Current										
(8233)	-20		-70	mA	5V	5V	0V	0V	0V	
Input Clamp Voltage										
A_n			-1.5	V	-12mA					
B_n			-1.5	V		-12mA				
S_0			-1.5	V			-12mA			
S_1			-1.5	V				-12mA		

$T_A = 25°C$ and $V_{CC} = 5.0V$

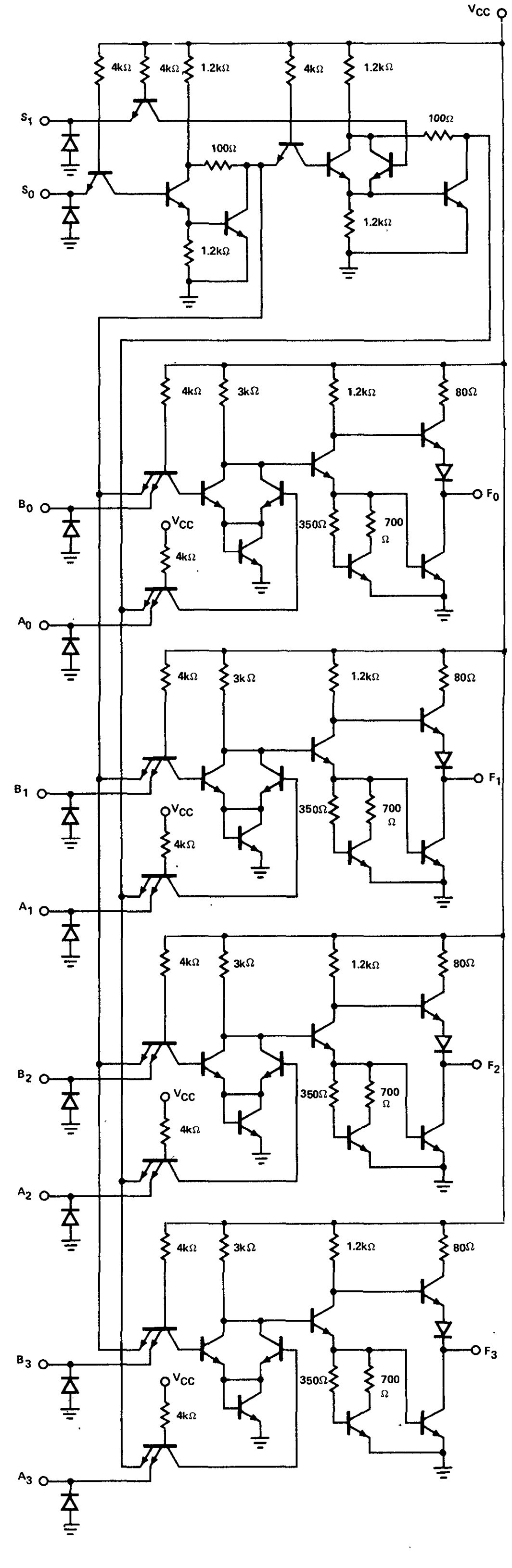
CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					INPUTS					
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1		
Power/Current										
Consumption:										
8233		200/38	252/48	mW/mA		0V		0V		15
8234		160/31	210/40	mW/mA		0V		0V		15
8235		230/44	310/59	mW/mA		4.5V		4.5V		15
8233 Turn-On Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8233 Turn-Off Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8234 Turn-On Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8234 Turn-Off Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8235 Turn-On Times										
A_n to f_n		16	25	ns						8,14
B_n to f_n		24	35	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8235 Turn-Off Times										
A_n to f_n		16	25	ns						8,14
B_n to f_n		24	35	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14

NOTES:

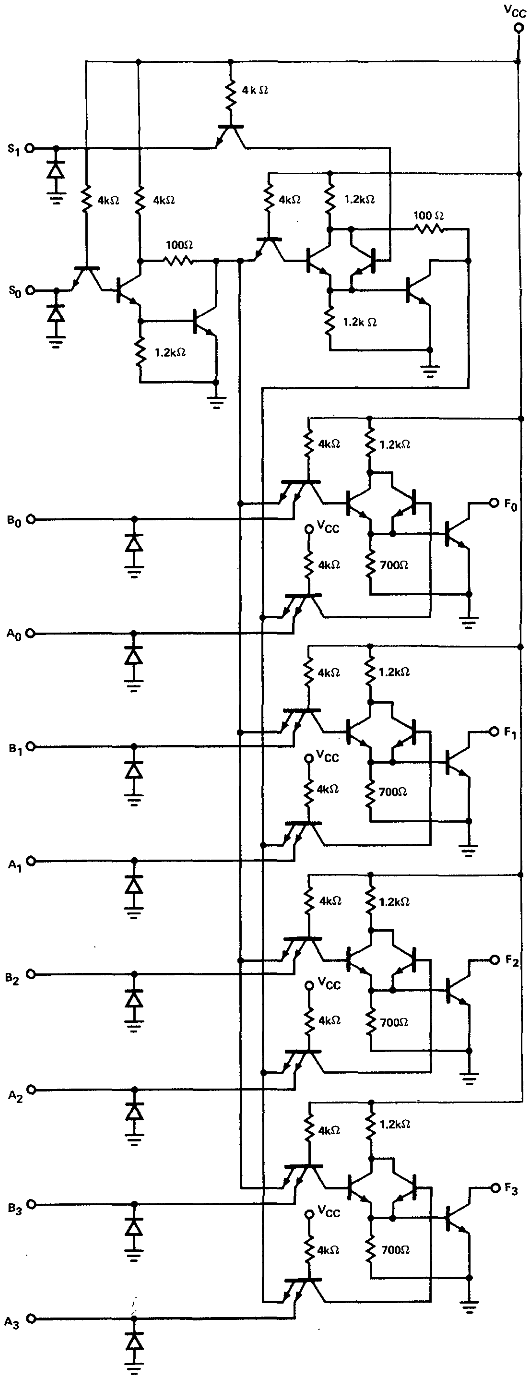
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. One DC fan-out is defined as 0.8mA.
9. One AC fan-out is defined as 50pF.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. This test guarantees operation free of input latch-up within the specified operating supply voltage range.
12. Measurements apply to each gate element independently.
13. Connect an external 1k ±1% resistor from V_{CC} to the output for this test.
14. Reference AC Test Circuit, Waveforms and Test Tables.
15. $V_{CC} = 5.25V$.

SCHEMATIC DIAGRAMS

8233

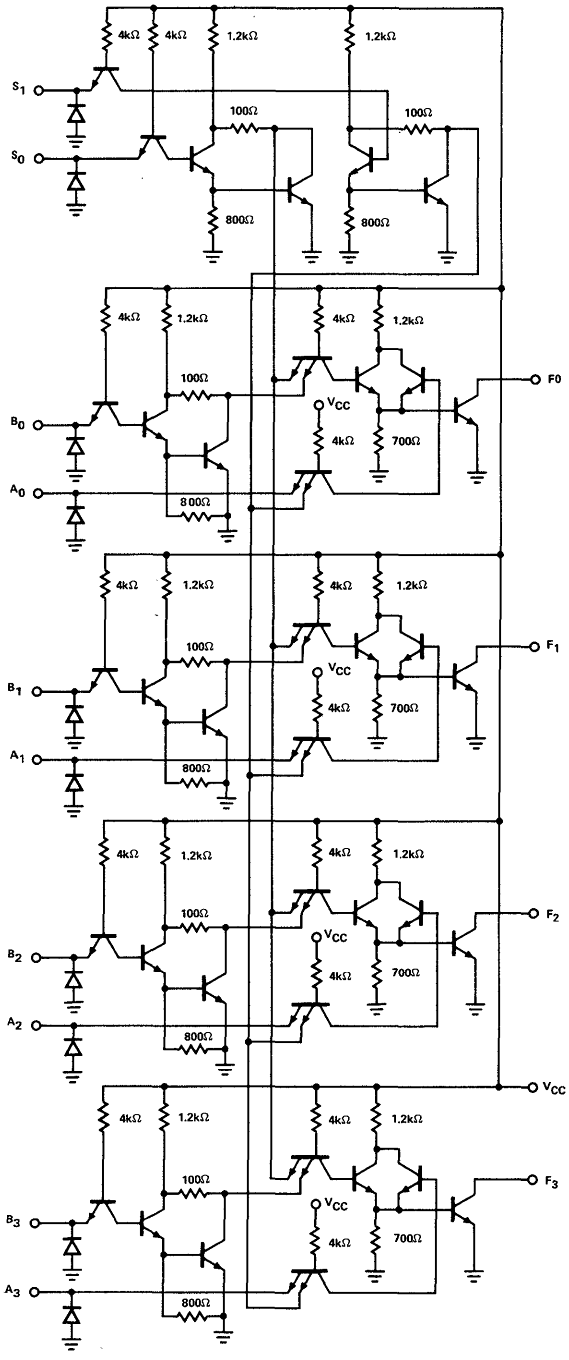


8234



SCHEMATIC DIAGRAMS (Cont'd)

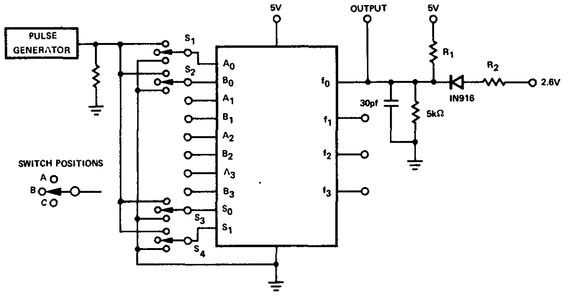
8235



PROPAGATION DELAY TEST TABLE

PRODUCT	PATH	PARAMETER	S_1	S_2	S_3	S_4
ALL	A_0 to f_0	t_{on} t_{off}	a	b	b	c
8233 8234	B_0 to f_0	t_{on} t_{off}	c	a	c	b
8233 8234	S_0 to f_0	t_{on} t_{off}	b	b	a	b
8233 8234	S_0 to f_0	t_{on} t_{off}	b	c	a	c
8235	B_0 to f_0	t_{on} t_{off}	c	a	c	b
8235	B_0 to f_0	t_{on} t_{off}	b	c	a	b
8235	S_1 to f_0	t_{on} t_{off}	b	b	c	a
8233 8234	S_1 to f_0	t_{on} t_{off}	b	c	b	a

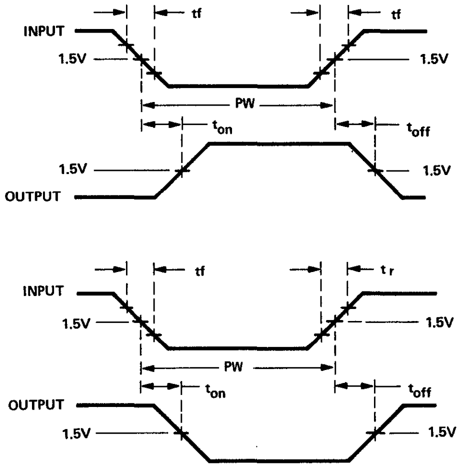
AC TEST FIGURE AND WAVEFORMS



	R_1	R_2
8233	∞	84.5Ω
8234 8235	360Ω	440Ω

INPUT PULSE:
Amplitude = 2.6V
PW = 200ns
PRR = 1 MHz
$t_r = t_f = 5ns$

PULSE REQUIREMENTS



QUAD EXCLUSIVE-OR
QUAD EXCLUSIVE-NOR

8241
8242

DIGITAL 8000 SERIES TTL/MSI

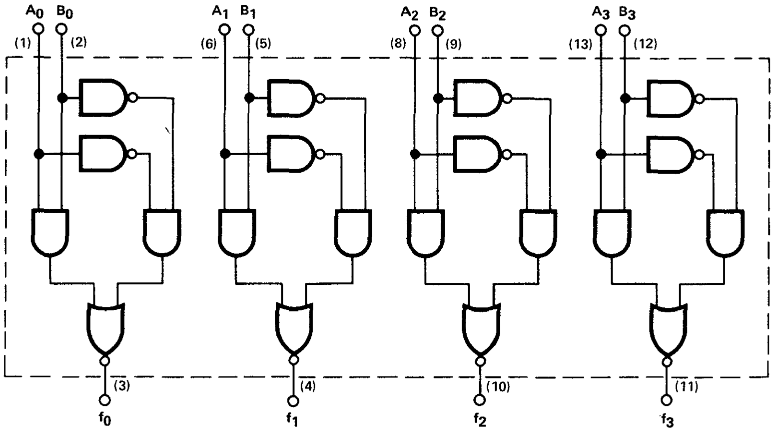
DESCRIPTION

The 8241 contains four independent gating structures to perform the Exclusive-OR function on two input variables. The output of the 8241 employs the totem-pole structure characteristic of TTL devices.

The 8242 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 8242 outputs are bare collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

LOGIC DIAGRAMS AND TRUTH TABLES

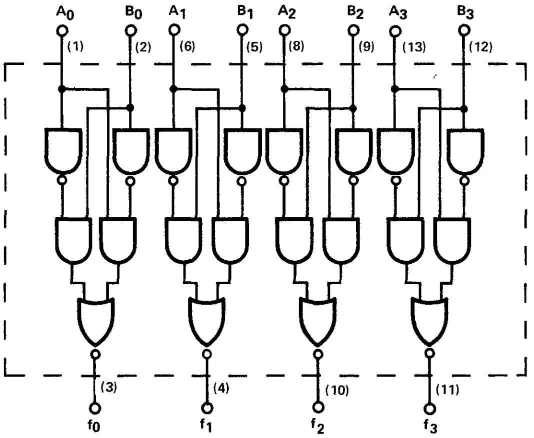
8241 QUAD EXCLUSIVE – OR



A	B	f
0	0	0
1	0	1
0	1	1
1	1	0

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

8242 4-BIT DIGITAL COMPARATOR



A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage) (8241)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS		OUTPUTS	
					A	B		
Output "1" Voltage	2.6	3.5		V	2.0	0.8	800μA	7
Output "0" Voltage			0.4	V	2.0	2.0	16mA	8
Input "1" Current			80	μA	4.5	4.5V		13
Input "0" Current	-0.1		-3.2	mA	0.4	0.4		14
Power/Current Consumption		225/42.4	300/57.1	mW/mA				
Output Short Circuit Current	-20		-70	mA			0V	6
Input Latch Voltage								
A Input	5.5			V	10mA	0V		10
B Input	5.5			V	0V	10mA		10

T_A = 25° C and V_{CC} = 5.0V (8241)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS		OUTPUTS	
					A	B		
Propagation Delay		12	20	ns				9

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage) (8242)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS		OUTPUT	
					A	B		
Output "1" Leakage Current			25	μA	2.0	2.0		12
Output "0" Voltage			0.4	V	2.0	0.8	25mA	8
Input "1" Current			80	μA	4.5	4.5V		13
Inpute "0" Current	-0.1		-3.2	mA	0.4	0.4		14
Power/Current Consumption		170/32	250/47.5	mW/mA	0.4	0.4		15
Input Latch Voltage								
A Input	5.5			V	10mA	0V		
B Input	5.5			V	0V	10mA		10

T_A = 25° C and V_{CC} = 5.0V (8242)

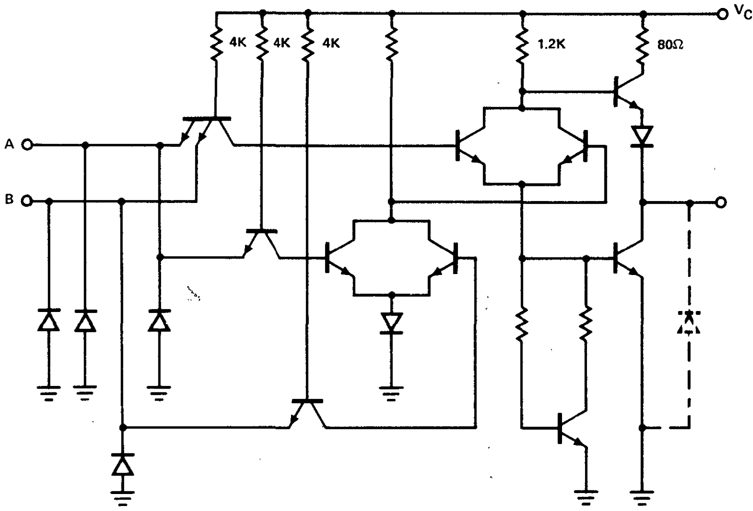
CHARACTERISTICS	LIMITS				TEST CONDITIONS			INPUTS
	MIN.	TYP.	MAX.	UNITS	INPUTS		OUTPUTS	
					A	B		
Propagation Delay		18	25	ns				9

NOTES:

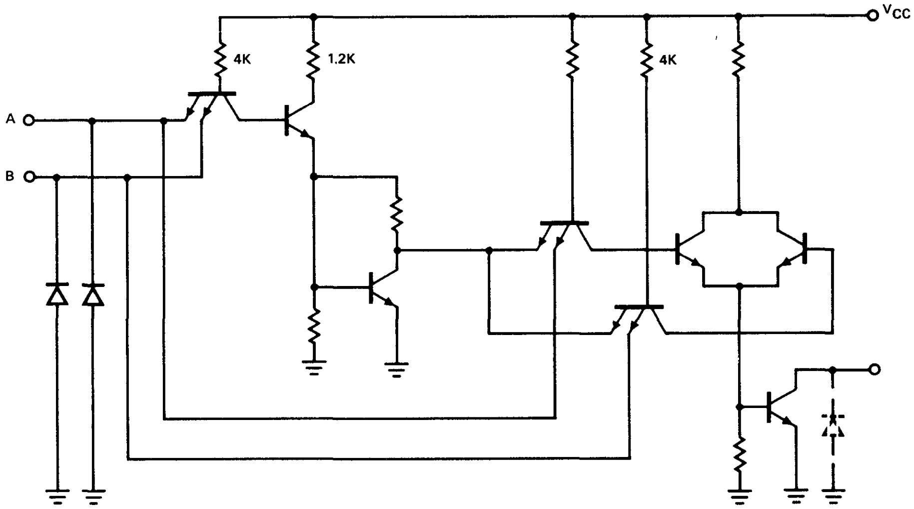
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
11. Manufacturers reserves the right to make design and process changes and improvements.
12. Connect an external 1K ±1% resistor from V_{CC} to the output terminal for this test.
13. A and B are tested separately. When A is 4.5V, B is 0V, and vice versa.
14. A and B are tested separately. When A is 0.4V, B is 5.25V, and vice versa.
15. V_{CC} = 5.25V.

SCHEMATIC DIAGRAMS

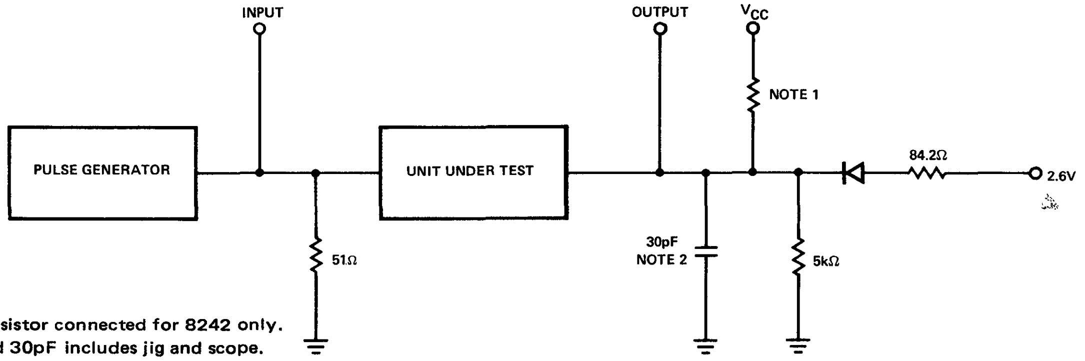
8241



8242

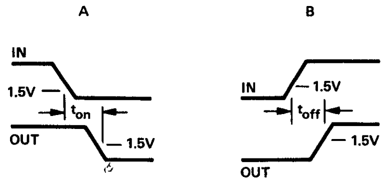


AC TEST FIGURE AND WAVEFORMS

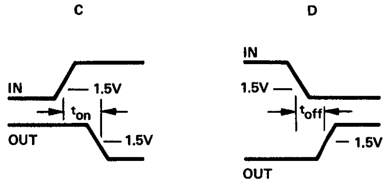


NOTE:
1. 530Ω resistor connected for 8242 only.
2. 5kΩ and 30pF includes jig and scope.

NON-INVERTING PATHS

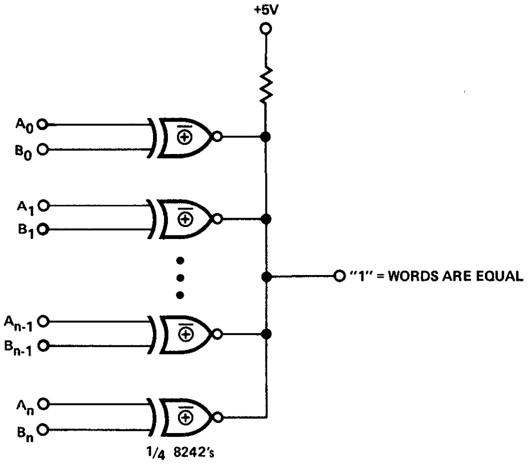


INVERTING PATHS

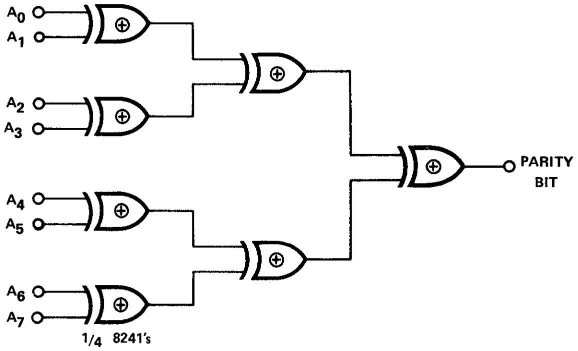


TYPICAL APPLICATIONS

EQUALITY GATE USED FOR COMPARISON



PARITY GENERATOR/TESTER



8-BIT POSITION SCALER

8243

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8243 8-Bit Position Scaler is an MSI array of approximately 70 gate complexity. The primary function of the 8243 is to scale (or shift) data bit positions by a selection of a 3-bit binary selector code.

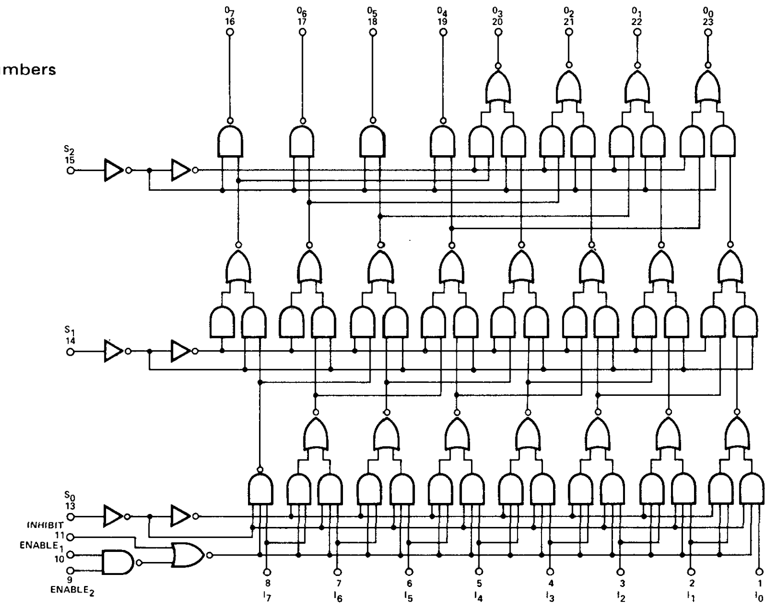
The most significant bit input (I_7) may be shifted 8 positions to the least significant bit output (O_0). At zero shift, or scale select, all eight input data bits are transferred and inverted to their respective outputs, (I_0 to O_0, I_1 to O_1, I_2 to O_2, etc.) At a shift, or scale select, of one, each input bit (I_n) will shift to the next lower output bit (O_{n-1}). See truth table for other shift codes.

The 8243's advantages over shift registers are the speed of operation and lower complexity of external logic required to effect a scale function. The speed of the 8243 Scaler is a function of gate propogation delays—the speed of equivalent shift registers is the time for clock periods plus the propagation delay to effect a scale function.

The 8243 is provided with open collector outputs to provide expansion to larger scaling functions. Data input logic zero loading is reduced to less than −100μA when the unit is disabled.

LOGIC DIAGRAM AND TRUTH TABLE

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers



NOTE: All inputs have diode clamps.

INHIBIT	ENABLE 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	1	0	0	0	$\overline{I_0}$	$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$
0	1	1	0	0	$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	1
0	1	0	1	0	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	1	1
0	1	1	1	0	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	1	1	1
0	1	0	0	1	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	1	1	1	1
0	1	1	0	1	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	1	1	1	1	1
0	1	0	1	1	$\overline{I_6}$	$\overline{I_7}$	1	1	1	1	1	1
0	1	1	1	1	$\overline{I_7}$	1	1	1	1	1	1	1
1	X	X	X	X	1	1	1	1	1	1	1	1
X	0	X	X	X	1	1	1	1	1	1	1	1

X Indicates either logic "1" or logic "0" may be present.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	I_n	S_0	S_1	S_2	ENABLE 1&2	INHIBIT	OUTPUTS	
"1" Output Leakage Current			150	µA	0.8V	*	*	*	2.0V	0.8V		7
"0" Output Voltage			0.4	V	2.0V	*	*	*	2.0V	0.8V	12.8mA	7
"0" Input Current												
Data In (Disabled)			-100	µA	0.4V				0.8V	2.0V		
Data In (Enabled)	-0.1		-1.6	mA	0.4V	0.8V			2.0V	0.8V		
Select S_n	-0.1		-1.6	mA		0.4V	0.4V	0.4V				
Inhibit	-0.1		-1.6	mA					0.4V	0.4V		
Enable 1 & 2	-0.1		-1.6	mA					0.4V	4.5V		11
"1" Input Current												
Data In			80	µA	4.5V	2.0V				2.0V		
Select S_n			40	µA		4.5V	4.5V	4.5V				
Inhibit			40	µA					2.0V	4.5V		
Enable 1 & 2			40	µA					4.5V			12

$T_A = 25°C$ and $V_{CC} = 5.0V$

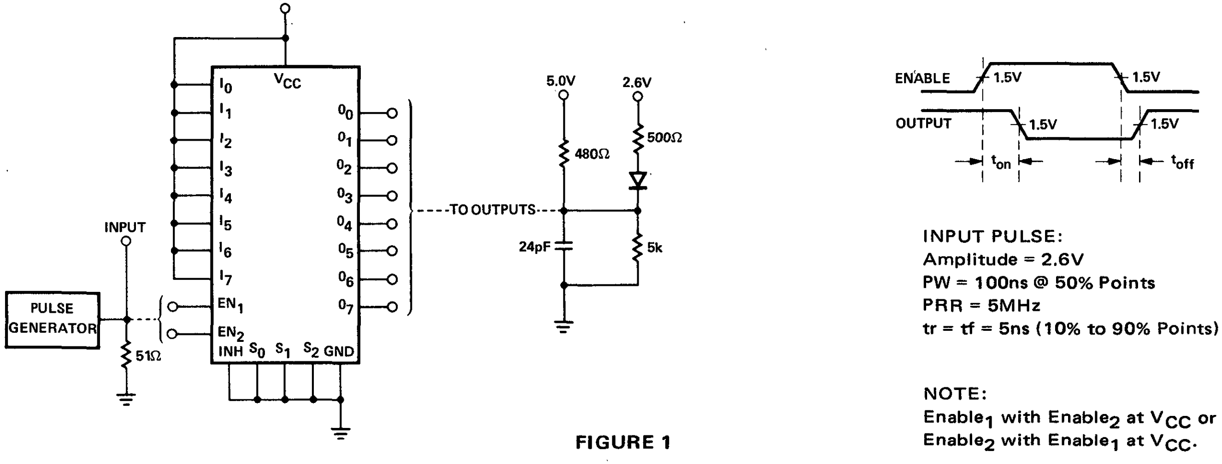
CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	I_n	S_0	S_1	S_2	ENABLE 1&2	INHIBIT	OUTPUTS	
Propagation Delay												
Data In		20	32	ns								9, 10
Select S_n		30	40	ns								
Inhibit		25	35	ns								
Enable 1 & 2		30	45	ns								
Power/Current Consumption		315/ 60	500/ 75.2	mW/ mA								13
Input Voltage Rating	5.5				10mA	10mA	10mA	10mA	10mA	10mA		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
8. Manufacturer reserves the right to make design and process changes and improvements.
9. Refer to AC Test figures.
10. I_n "0" threshold 0.7 volts for S8243.
11. Input under test at 0.4V, other Enable Input tied to V_{CC}.
12. Input under test at 4.5V, other Enable Input, 0 volts.
13. V_{CC} = 5.25V.

AC TEST FIGURES AND WAVEFORMS

PROPAGATION DELAY, ENABLE TO OUTPUT



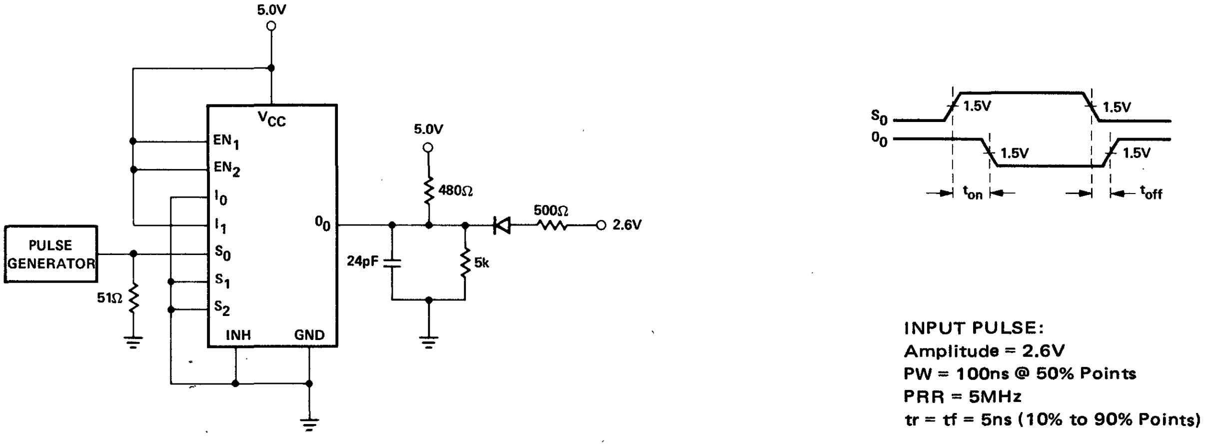
INPUT PULSE:
Amplitude = 2.6V
PW = 100ns @ 50% Points
PRR = 5MHz
tr = tf = 5ns (10% to 90% Points)

NOTE:
$Enable_1$ with $Enable_2$ at V_{CC} or $Enable_2$ with $Enable_1$ at V_{CC}.

FIGURE 1

AC TEST FIGURES AND WAVEFORMS (Cont'd)

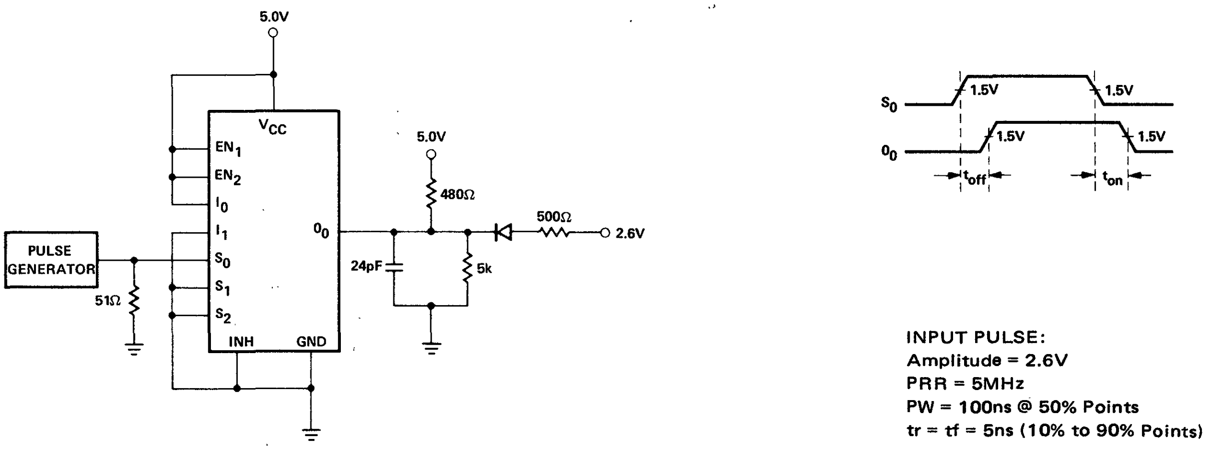
PROPAGATION DELAY, DATA INPUT TO DATA OUTPUT



INPUT PULSE:
Amplitude = 2.6V
PW = 100ns @ 50% Points
PRR = 5MHz
tr = tf = 5ns (10% to 90% Points)

FIGURE 2

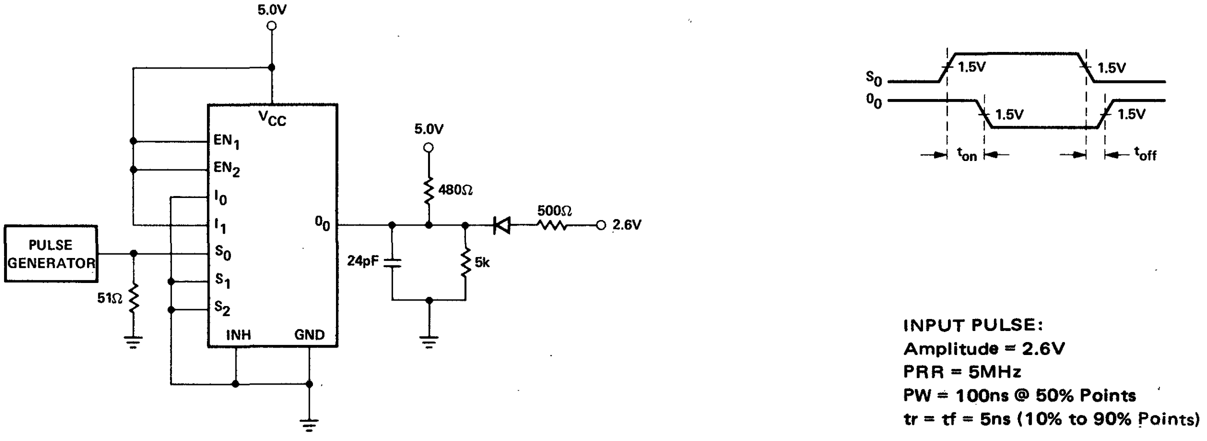
PROPAGATION DELAY, DATA SELECT TO OUTPUT



INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz
PW = 100ns @ 50% Points
tr = tf = 5ns (10% to 90% Points)

FIGURE 3

PROPAGATION DELAY, DATA SELECT TO OUTPUT

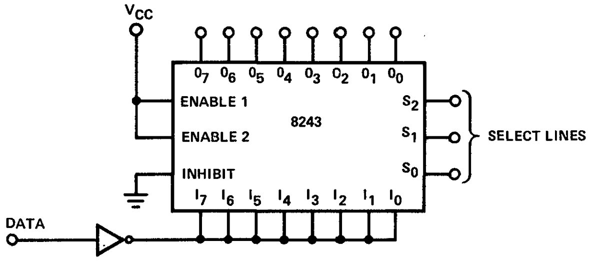


INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz
PW = 100ns @ 50% Points
tr = tf = 5ns (10% to 90% Points)

FIGURE 4

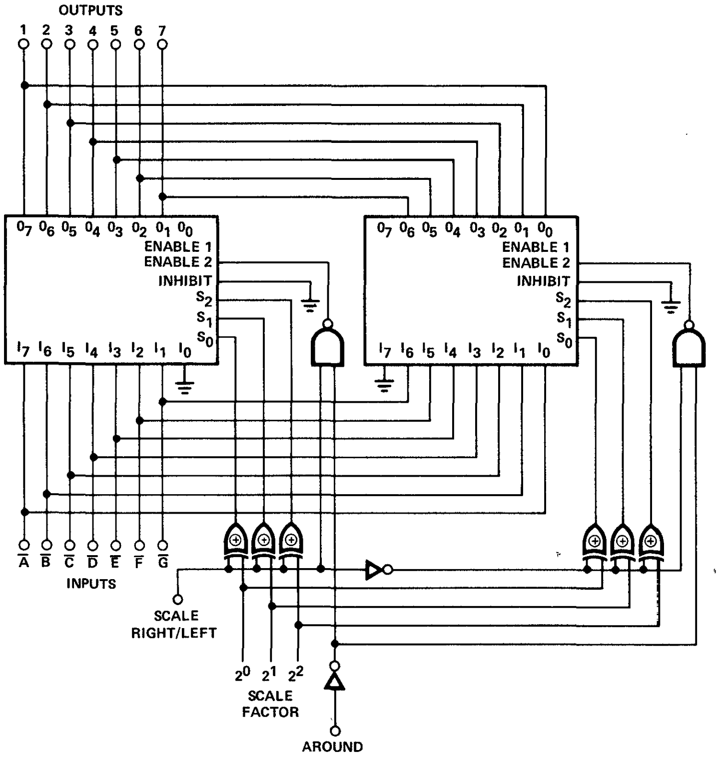
TYPICAL APPLICATIONS

ONE TO EIGHT LINE DEMULTIPLEXER



SCALE SELECT	3 BIT BINARY CODE			OUTPUTS							
	S_2	S_1	S_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	0	Data	Data	Data	Data	Data	Data	Data	Data
1	0	0	1	Data	Data	Data	Data	Data	Data	Data	1
2	0	1	0	Data	Data	Data	Data	Data	Data	1	1
3	0	1	1	Data	Data	Data	Data	Data	1	1	1
4	1	0	0	Data	Data	Data	Data	1	1	1	1
5	1	0	1	Data	Data	Data	1	1	1	1	1
6	1	1	0	Data	Data	1	1	1	1	1	1
7	1	1	1	Data	1	1	1	1	1	1	1

BI-DIRECTIONAL 8-POSITION SHIFTER



SCALE FACTOR	OUTPUTS							
	1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	1	A	B	C	D	E	F	RIGHT
2	1	1	A	B	C	D	E	
3	1	1	1	A	B	C	D	
4	1	1	1	1	A	B	C	
5	1	1	1	1	1	A	B	SCALE = 0
6	1	1	1	1	1	1	A	AROUND = 0
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS							
	1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	B	C	D	E	F	G	1	LEFT
2	C	D	E	F	G	1	1	
3	D	E	F	G	1	1	1	
4	E	F	G	1	1	1	1	
5	F	G	1	1	1	1	1	SCALE = 1
6	G	1	1	1	1	1	1	AROUND = 0
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS							
	1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	G	A	B	C	D	E	F	RIGHT
2	F	G	A	B	C	D	E	& AROUND
3	E	F	G	A	B	C	D	
4	D	E	F	G	A	B	C	
5	C	D	E	F	G	A	B	SCALE = 0
6	B	C	D	E	F	G	A	AROUND = 1
7	A	B	C	D	E	F	G	

SCALE FACTOR	OUTPUTS							
	1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	B	C	D	E	F	G	A	LEFT
2	C	D	E	F	G	A	B	& AROUND
3	D	E	F	G	A	B	C	
4	E	F	G	A	B	C	D	
5	F	G	A	B	C	D	E	SCALE = 1
6	G	A	B	C	D	E	F	AROUND = 1
7	A	B	C	D	E	F	G	

BINARY-TO-OCTAL DECODER
BCD-TO-DECIMAL DECODER

8250
8251
8252

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8250, 8251 and 8252 are gate arrays for decoding and logic conversion applications.

The 8250 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

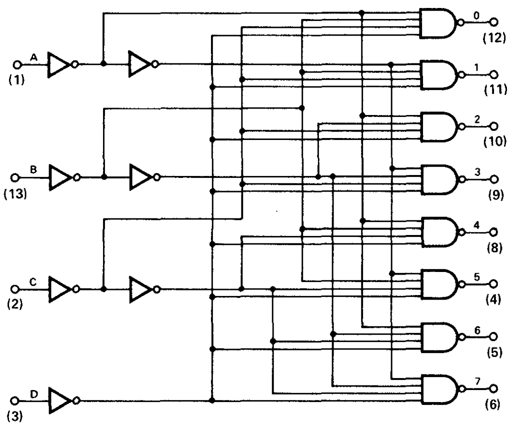
The 8251 and 8252 convert a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

The 8252 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs.

The selected output is a logic "0".

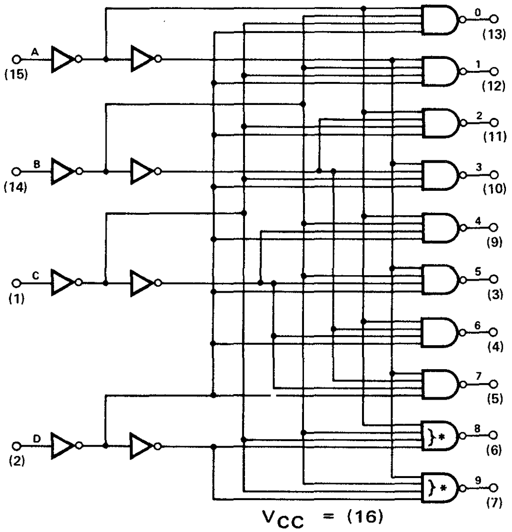
LOGIC DIAGRAMS

8250



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

8251/8252



V_{CC} = (16)
GND = (8)
*Connections made on 8252 only ( ) = Denotes Pin Numbers

TRUTH TABLE

INPUT STATE				OUTPUT STATES											
				8250								8251		8252	
A	B	C	D	0	1	2	3	4	5	6	7	8	9	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0
0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS						
"1" Output Voltage	2.6	3.5		V					-800	6, 10
"0" Output Voltage			0.4	V					16mA	7, 10
"1" Input Current A, B, C, D			40	μA	4.5V	4.5V	4.5V	4.5V		
"0" Input Current A, B, C (8250, 8251)	-0.1		-1.2	mA	0.4V	0.4V	0.4V			
A, B, C, D (8252)	-0.1		-1.6	mA	0.4V	0.4V	0.4V	0.4V		
D (8251 Only)	-0.1		-1.2	mA				0.4V		
D (8250 Only)	-0.1		-1.0	mA				0.4V		

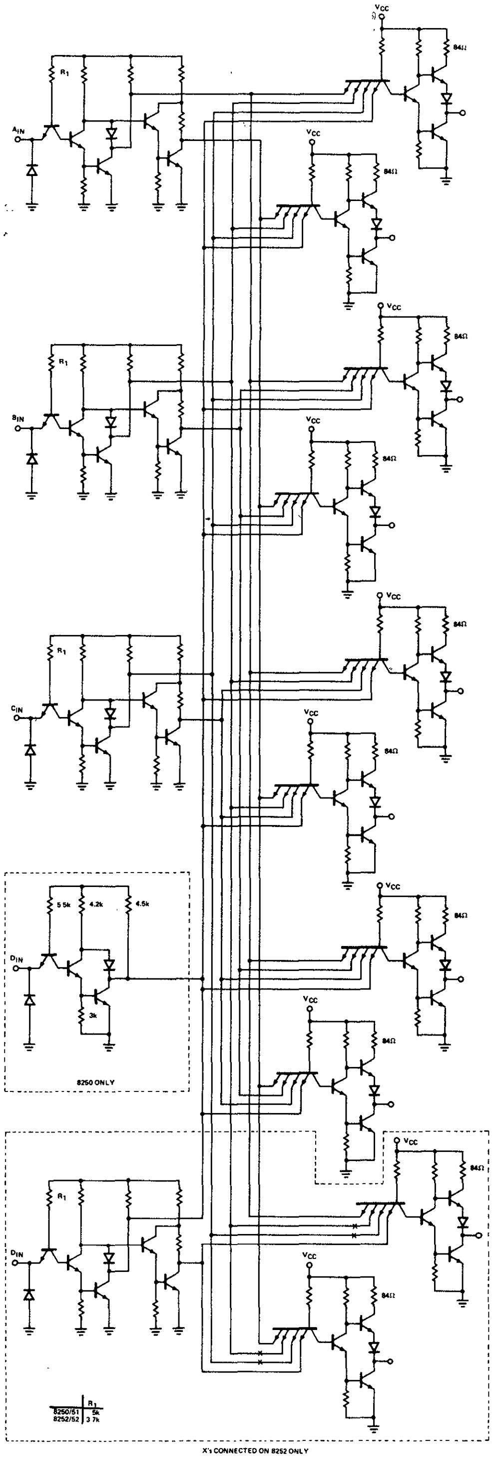
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS						
Turn-on Delay t_{on}		20	35	ns						8
Turn-off Delay t_{off}		20	35	ns						8
Power/Current Consumption (8251 Only)			135/25.7	mW/mA	5.25V	5.25V	5.25V	0V		12
(8250 Only)			125/23.8	mW/mA	5.25V	5.25V	5.25V	0V		12
Input Latch Voltage	5.5			V	10mA	10mA	10mA	10mA		11
Output Short Circuit Current Outputs 1 thru 9	-10		-55	mA	0V	0V	0V	0V	0V	
Output 0	-10		-55	mA	5.0V	0V	0V	0V	0V	

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1". "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Inputs for "1" and "0" output voltage test is per TRUTH table with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM



AC TEST FIGURE AND WAVEFORMS

TURN-ON DELAY (t_{on})

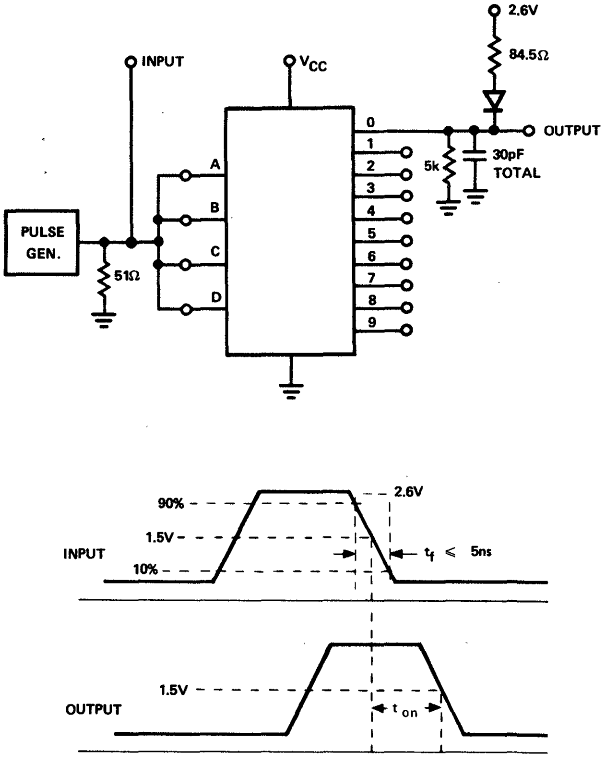
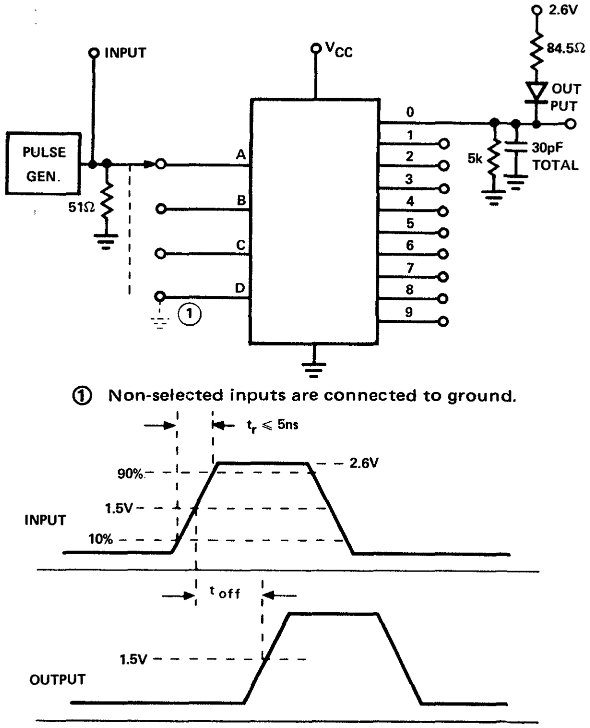


FIGURE 1

TURN-OFF DELAY (t_{off})

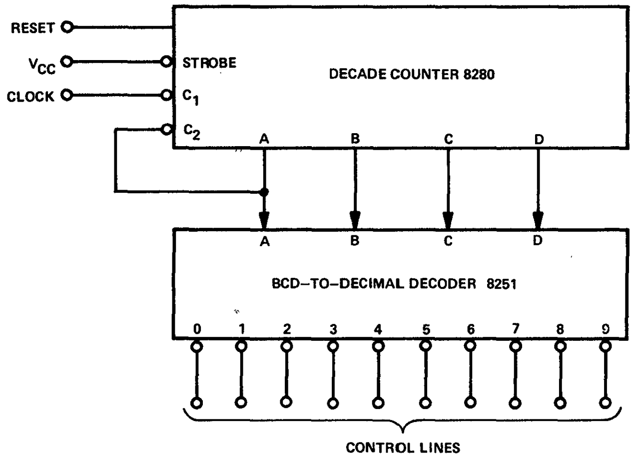


① Non-selected inputs are connected to ground.

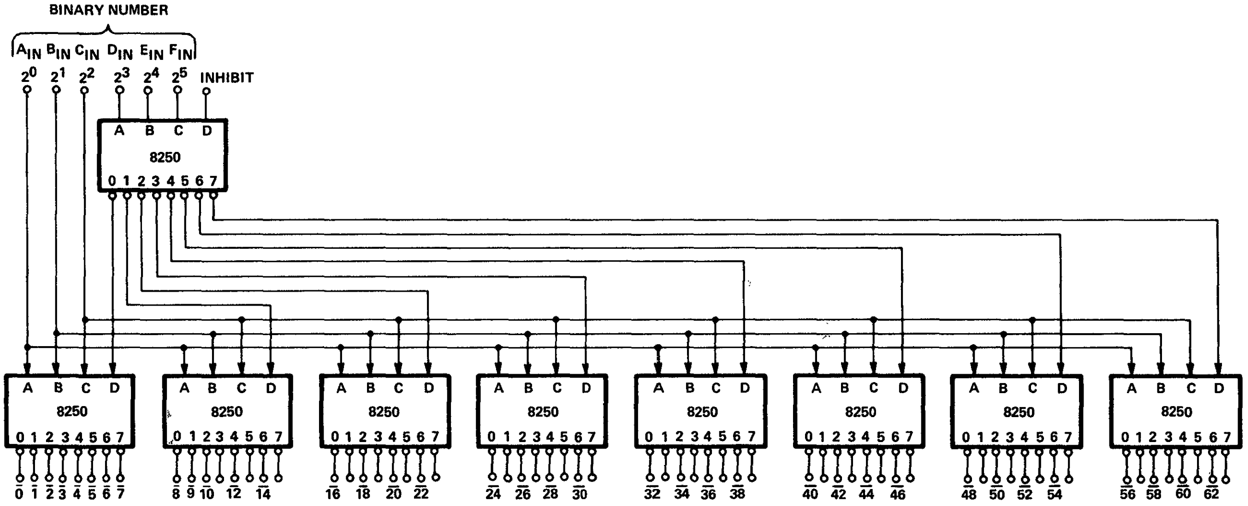
FIGURE 2

TYPICAL APPLICATIONS

ONE-OF-10 DECODER



ONE-OF-64 DECODER



ARITHMETIC LOGIC ELEMENT 8260

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

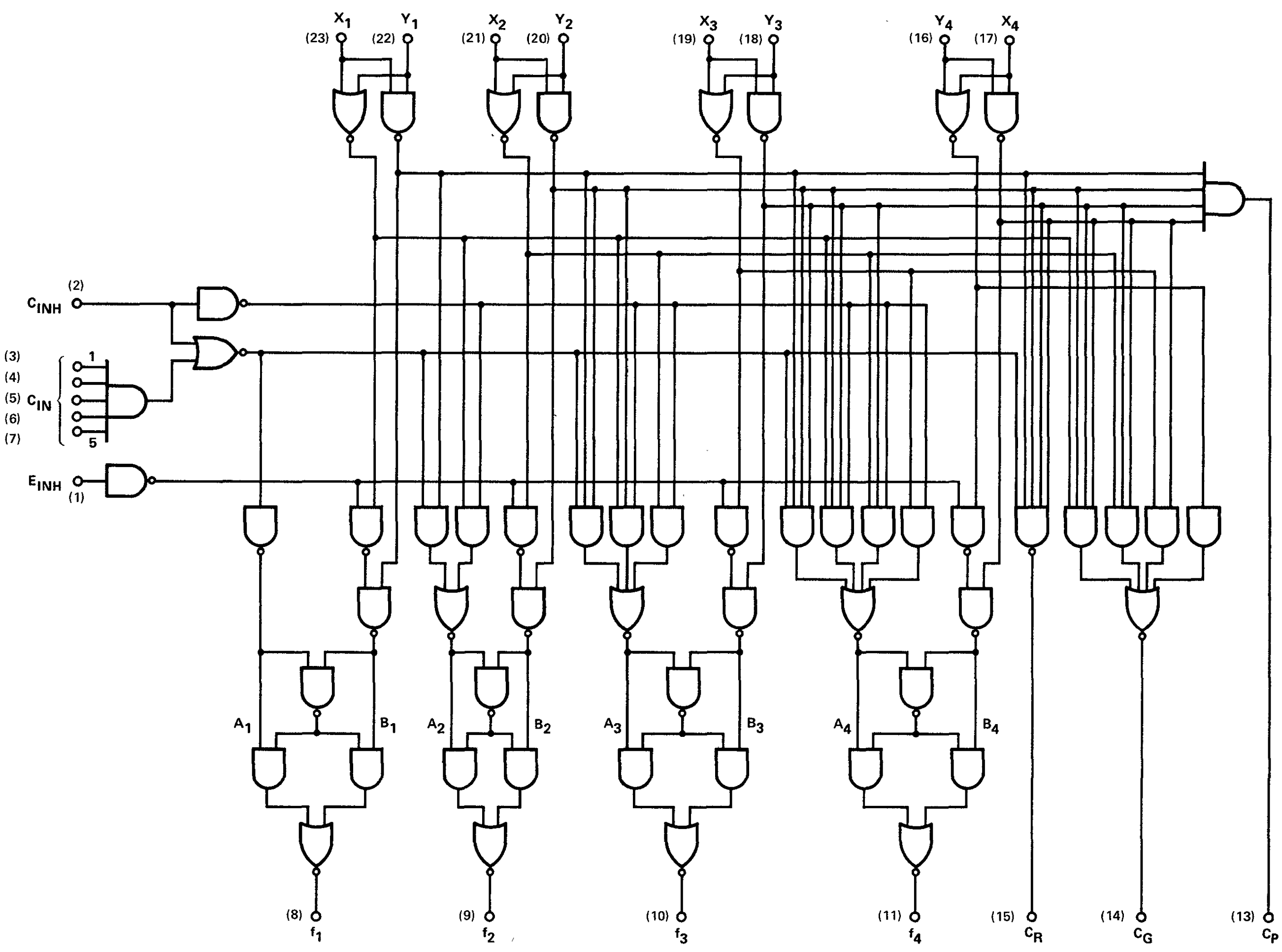
The 8260 Arithmetic Logic Element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. The device may be used as four mutually independent exclusive NOR or AND gates by proper addressing of the inhibit lines.

As a four-bit adder, the 8260 permits high speed parallel addition of four sets of data and features both simultaneous addition on a character to character and on a bit to bit basis within the package.

When true input variables are used, the true sum is formed at the f output. Inverted input variables produce the complement of the sum of the true variables.

The carry-outs available are: Internally Generated (C_G); Propagated (C_p); and Ripple (C_R). This gives the 8260 complete flexibility when used in Ripple Carry or Anticipated Carry Adder Systems.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (12)
( ) = Denotes Pin Numbers
A and B refer to Functional Block Diagram on page 54.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUT TERMINALS					OUTPUT TERMINALS (mA)				NOTES
	MIN.	TYP.	MAX.	UNITS	X_n	Y_n	C_{IN}	C_{INH}	E_{INH}	C_p	C_G	C_R	f_n	
"1" Output Voltage	2.6	3.5		V	2.0	2.0	2.0	2.0	2.0		-0.8	-0.8	-0.8	1
"0" Output Voltage														
f_n, C_G and C_R			0.4	V	0.8	0.8	0.8	0.8	0.8		9.6	9.6	9.6	2
"0" Input Current														
X_n and C_{INH}	-0.1		-3.2	mA	0.4	5.25		0.4						
Y_n	-0.1		-3.2	mA	5.25	0.4								
E_{INH} & C_{IN1}, through C_{IN5}	-0.1		-1.6	mA			0.4		0.4					3
"1" Input Current														
X_n and C_{INH}			80	μA	4.5	0V		4.5						
Y_n			80	μA	0V	4.5								
E_{INH} & C_{IN1}, through C_{IN5}			40	μA			4.5		4.5					4
Input Latch Voltage														
X_n and C_{INH}	5.5			V	10mA	0V		10mA						
Y_n	5.5			V	0V	10mA								
E_{INH} & C_{IN1}, through C_{IN5}	5.5			V			10mA		10mA					4
Power/Current Consumption			400/ 76.2	600/ 114.1	mW/ mA									15

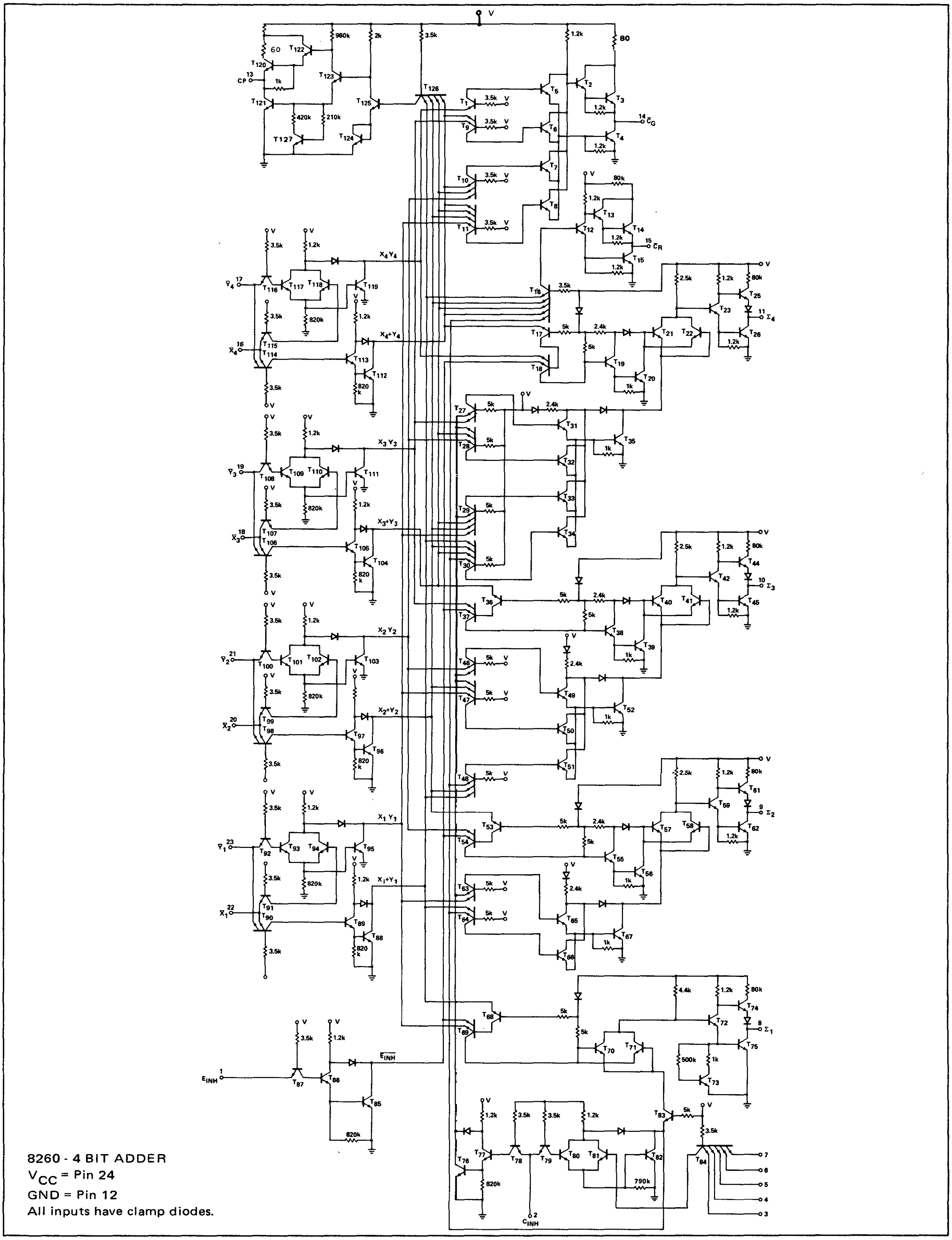
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUT TERMINALS					OUTPUT TERMINALS (mA)				NOTES
	MIN.	TYP.	MAX.	UNITS	X_n	Y_n	C_{IN}	C_{INH}	E_{INH}	C_p	C_G	C_R	f_n	
Propagation Delay														
X_n, Y_n and C_{IN} to C_R		14	20	ns										14
X_n and Y_n to Cp and C_G		14	20	ns										14
X_n and Y_n to f_n		24	33	ns										14
C_{IN} to f_n		14	22	ns										14
Output Short Circuit Current														
f_n, C_G and C_R	-20		-70	mA	5.0	5.0	5.0	5.0	5.0		0V	0V	0V	13
Cp	-40		-90	mA	0V					0V				

NOTES:

1. Output source current is supplied through a resistor to ground.
2. Output sink current is supplied through a resistor to V_{CC}.
3. When testing for separate C_{IN} inputs, tie the remaining C_{IN} inputs to V_{CC}.
4. When testing for separate C_{IN} inputs, tie the remaining C_{IN} inputs to ground.
5. Keep unused inputs tied to V_{CC} unless otherwise specified.
6. All voltage and capacitance measurements are referenced to the ground terminal.
7. All measurements are taken with ground pin tied to "0" volts.
8. Positive current flow is defined as into the terminal referenced.
9. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
10. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. Input latch voltage test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. Ground one output at a time.
14. Measure switching times at 1.5 volt level.
15. $V_{CC} = 5.25V$.

SCHEMATIC DIAGRAM



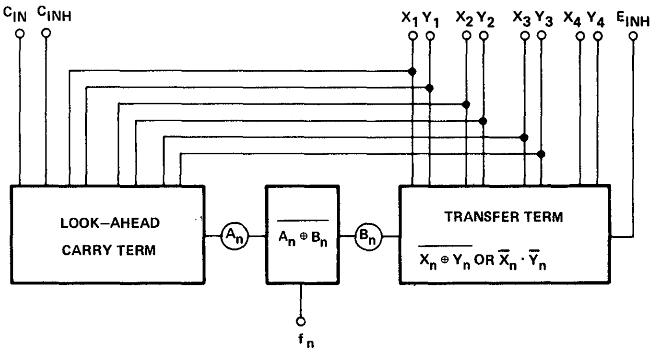
8260 - 4 BIT ADDER
V_{CC} = Pin 24
GND = Pin 12
All inputs have clamp diodes.

MODE OF OPERATION

INPUTS	Least Significant C_{IN} Inputs to be *	CONTROLS		f	
		C_{INH}	E_{INH}		
X_n, Y_n	0	0	0	Σ_n	Add
	0	0	1	--	Not Used
	0	1	0	$X_nY_n + \overline{X}_n\overline{Y}_n$	Coincidence
	0	1	1	X_nY_n	AND
$\overline{X}_n$, $\overline{Y}_n$	1	0	0	$\overline{\Sigma}_n$	Add
	1	0	1	---	Not Used
	1	1	0	$\overline{X}_n\overline{Y}_n + X_nY_n$	Coincidence
	1	1	1	$\overline{X}_n\overline{Y}_n$	AND

*Least significant of a "Multiple Package" adder system.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

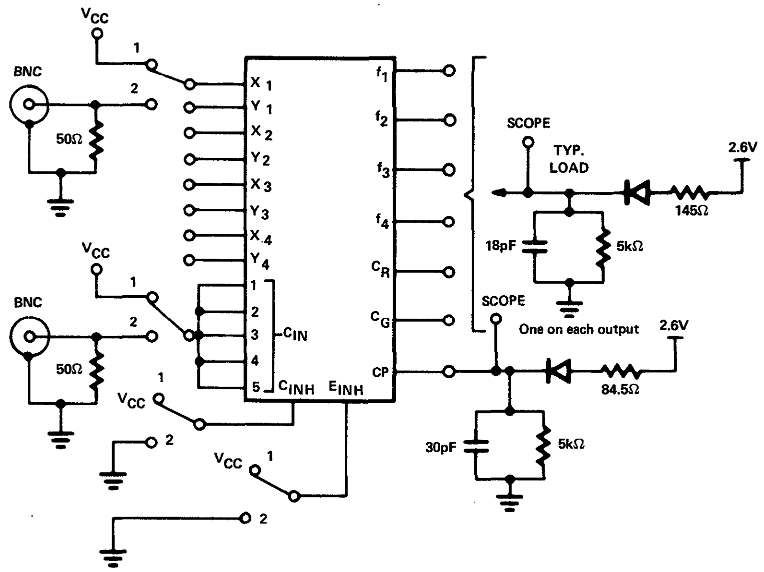
$C_{INH} = 1 \longrightarrow A_n = 1$
$C_{INH} = 0 \longrightarrow A_n =$

C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

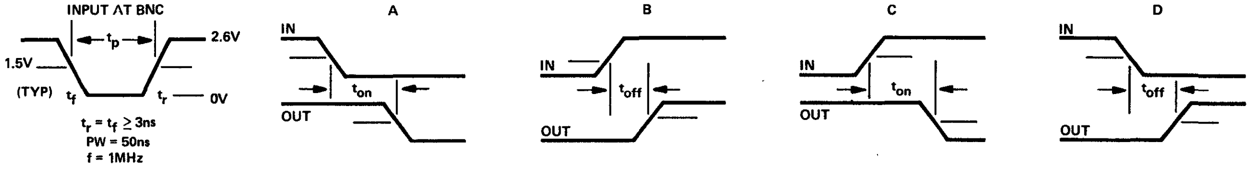
A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

AC TEST FIGURE AND WAVEFORMS



NOTE: Scope terminals to be ⩽ ½" from Package Pins.



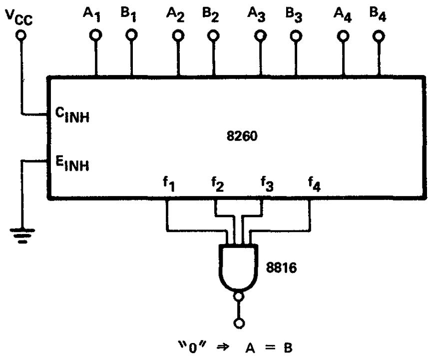
STEP NO.	DELAY FROM-TO	SWITCH POSITION												WAVEFORM TYPE
		DRIVEN INPUTS	OTHER INPUTS											
			X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	C_{IN}	E_{INH}	C_{INH}	
1	X_n to C_R or X_n to C_P	2	2	1	2	1	2	1	2	1	2	2	2	A, B C, D
2	Y_n to C_R or Y_n to C_P	2	1	2	1	2	1	2	1	2	2	2	2	A, B C, D
3	X_n,Y_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	A, B
4	C_{IN} to C_R	2	2	2	2	2	2	2	2	2	2	2	2	A, B
5	C_{IN} to f_n	2	1	2	1	2	1	2	1	2	2	2	2	C, D

TYPICAL APPLICATIONS

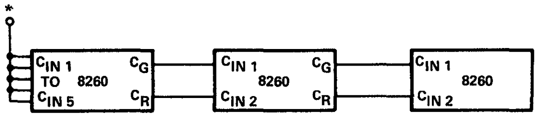
The 8260 contains the control logic necessary to allow operation as a general purpose arithmetic logic device. Below, the internal carries are inhibited to effect Exclusive-NOR or coincidence operation. The 8260 may also be operated as four independent AND gates to implement masking and similar requirements of micro-programming.

The Ripple Adder System is the simplest but also the slowest application of the 8260. The typical total addition time (input to sum output for 12-bit ripple adder is 42ns.).

FOUR-BIT COMPARATOR



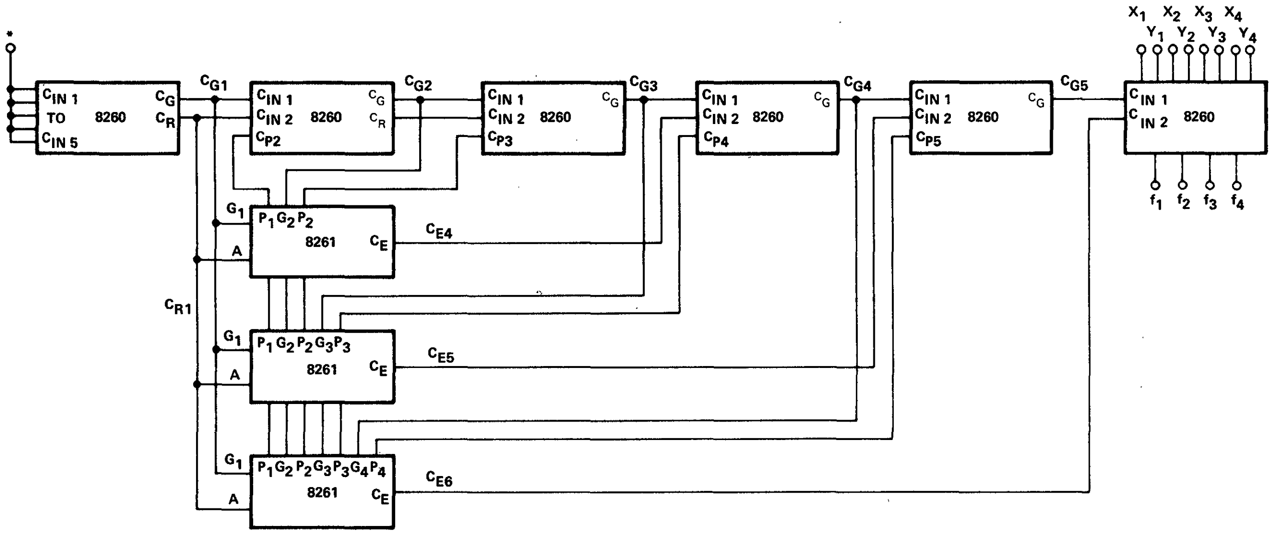
RIPPLE ADDER SYSTEM



*Tied to V_{CC} if Not-True Inputs Are Used, Otherwise to Ground.

The Fast Adder System provides complete carry look-ahead addition for words to 24 bits in length and is the fastest application of the 8260 units. The typical total addition time for a 24 bit fast adder is 42ns.

24-BIT FAST ADDER SYSTEM



*Tied to V_{CC} if Not-True Inputs Are Used, Otherwise to Ground.

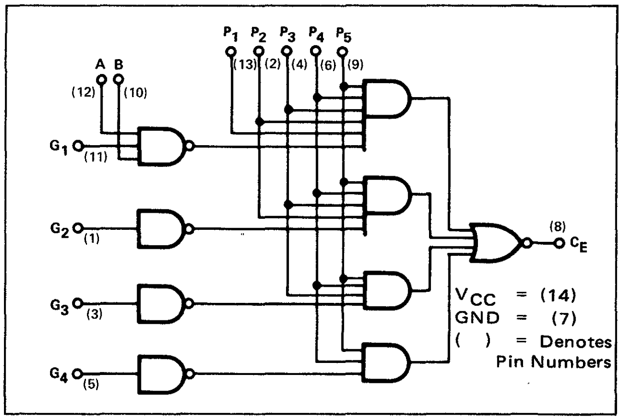
FAST CARRY EXTENDER 8261

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8261 Fast Carry Extender is a monolithic gate array designed specifically to be used in conjunction with the 8260 Arithmetic Logic element. A 8260/8261 combination facilitates the implementation of the look-ahead technique in adder systems, thus considerably improving propagation times. The circuit structure of this array is of the familiar TTL type.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					DRIVEN INPUTS		OTHER INPUTS			
	MIN.	TYP.	MAX.	UNITS	G,A,B	P	G,A,B	P		
"1" Output Voltage	2.6	3.5		V	2.0V				-800µA	6
"0" Output Voltage			0.4	V	0.8V		4.75V	4.75V	9.6mA	7
"1" Input Current										
G Input			40	µA	4.5V		A = 0V			
A and B Inputs			40	µA	4.5V		G_1 = 0V			
P_1 Input			40	µA		4.5V		0V		
P_2 Input			80	µA		4.5V		0V		
P_3 Input			120	µA		4.5V		0V		
P_4 and P_5 Inputs			160	µA		4.5V		0V		
"0" Input Current										
G, A and B			-1.6	mA	0.4V			5.25V		
P_1 Input			-1.6	mA		0.4V	0V	5.25V		
P_2 Input			-3.2	mA		0.4V	0V	5.25V		
P_3 Input			-4.8	mA		0.4V	0V	5.25V		
P_4 and P_5 Inputs			-6.4	mA		0.4V	0V	5.25V		
Power/Current Consumption		95/18.1	140/26.6	mW/mA			5.25V	0V		12
Input Latch Voltage	5.5			V	10mA	10mA	0V	0V		9

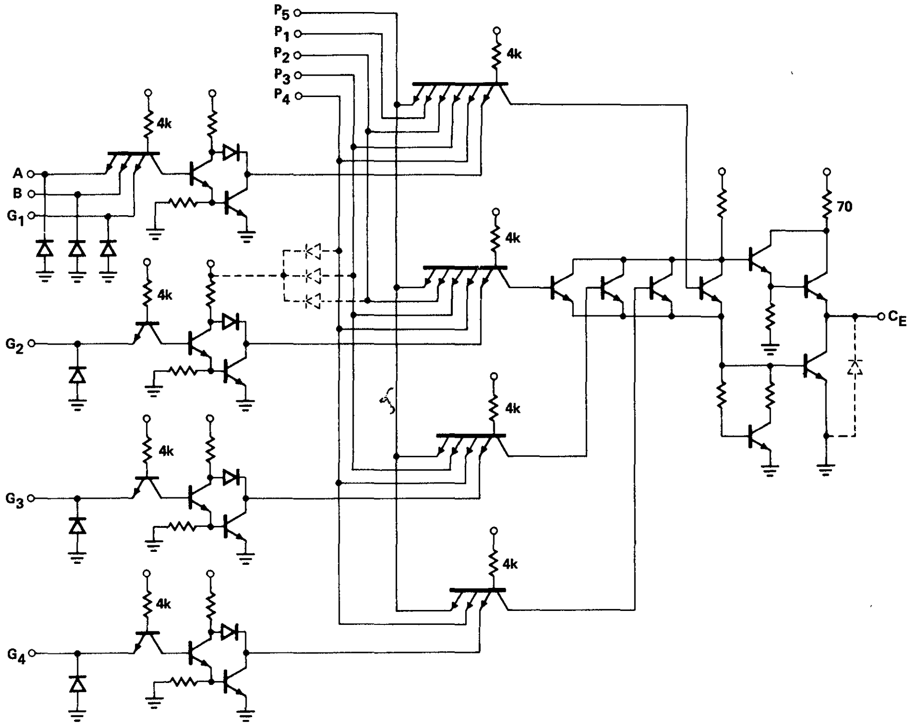
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					DRIVEN INPUTS		OTHER INPUTS			
	MIN.	TYP.	MAX.	UNITS	G,A,B	P	G,A,B	P		
Turn-on Delay										
G to C_E		12	18	ns						8
P to C_E		9	14	ns						8
Turn-off Delay										
G to C_E		11	16	ns						8
P to C_E		8	12	ns						8
Output Short Circuit Current	-20		-70	mA	5.0V	0V			0V	

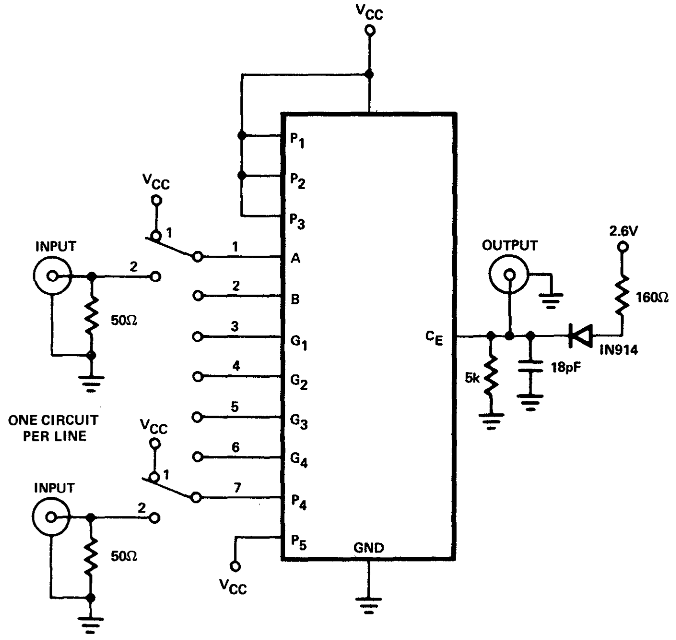
NOTES:

1. All voltage and current measurements are referenced to the ground terminal. Input terminals not specifically referenced are tied to V_{CC}.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. Input "0" thresholds for P_1 through P_5 inputs are guaranteed to be 0.7 volts.
12. V_{CC} = 5.25V.

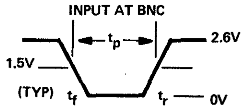
SCHEMATIC DIAGRAM



AC TEST FIGURE AND WAVEFORMS

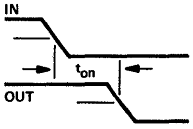


PIN DES. \ SWITCH NO.	SWITCH POSITION							WAVEFORM TYPE
	1	2	3	4	5	6	7	
A	2	1	1	1	1	1	1	A and B
B	1	2	1	1	1	1	1	
G1	1	1	2	1	1	1	1	
G2	1	1	1	2	1	1	1	
G3	1	1	1	1	2	1	1	
G4	1	1	1	1	1	2	1	
P4								
STEP A	2	1	1	1	1	1	2	C and D
STEP B	1	2	1	1	1	1	2	
STEP C	1	1	2	1	1	1	2	
STEP D	1	1	1	2	1	1	2	
STEP E	1	1	1	1	2	1	2	
STEP F	1	1	1	1	1	2	2	

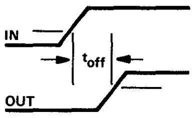


$t_r = t_f \geq 3ns$
PW = 50ns
f = 1MHz

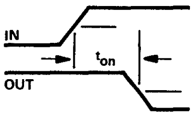
A



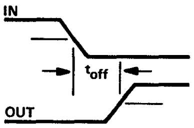
B



C



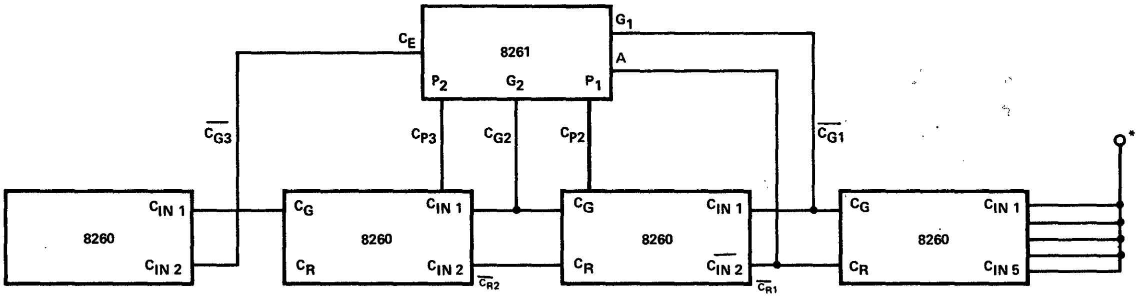
D



NOTES:

1. Scope terminals to be ⩽ 1-1/2" from package pins.
2. Position 1 on all switches provides a logical "1". Position 2 on all switches provides a logical "0" when input signal is not present.
3. All measurements are made at 1.5 volts level.

TYPICAL APPLICATION



16 BIT, T_A = 42ns, typical Fast Adder System (5 packages)
*Tied to V_{CC} if not-true inputs are used, otherwise to ground. Unused 8261 pins should be tied to V_{CC}.

9-BIT PARITY GENERATOR AND CHECKER

8262

DIGITAL 8000 SERIES TTL/MSI

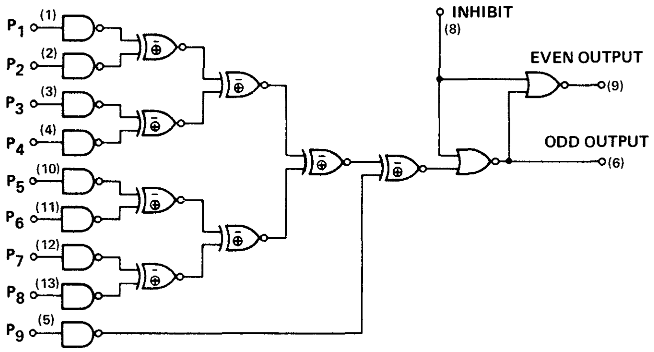
DESCRIPTION

The 8262 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 8262. (A logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a Parity Generator, the 8262 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the 8262 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

LOGIC EQUATIONS:

Odd =
$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

Even =
$\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT UNDER TEST			
"1" Output Voltage								
Even	2.6	3.5		V	0V	.8V	-800μA	6
Odd	2.6	3.5		V	2.0V	.8V	-800μA	6
"0" Output Voltage								
Even			0.40	V	2.0V	.8V	16mA	7
Odd			0.40	V	0V	.8V	16mA	7
"0" Input Current								
Data Inputs	-0.1		-1.6	mA	0.4V			
Inhibit	-0.1		-3.2	mA		0.4V		
"1" Input Current								
Data Inputs			80	μA	4.5V			
Inhibit			160	μA		4.5V		
Input Latch Voltage								
Data Inputs	5.5			V	10mA			10
Inhibit	5.5			V		10mA		10
Power/Current Consumption			370/70	mW/mA				11
Output Short Circuit Current								
Even	-20		-70	mA	0V	0V	0V	
Odd	-20		-70	mA	4.5V	0V	0V	

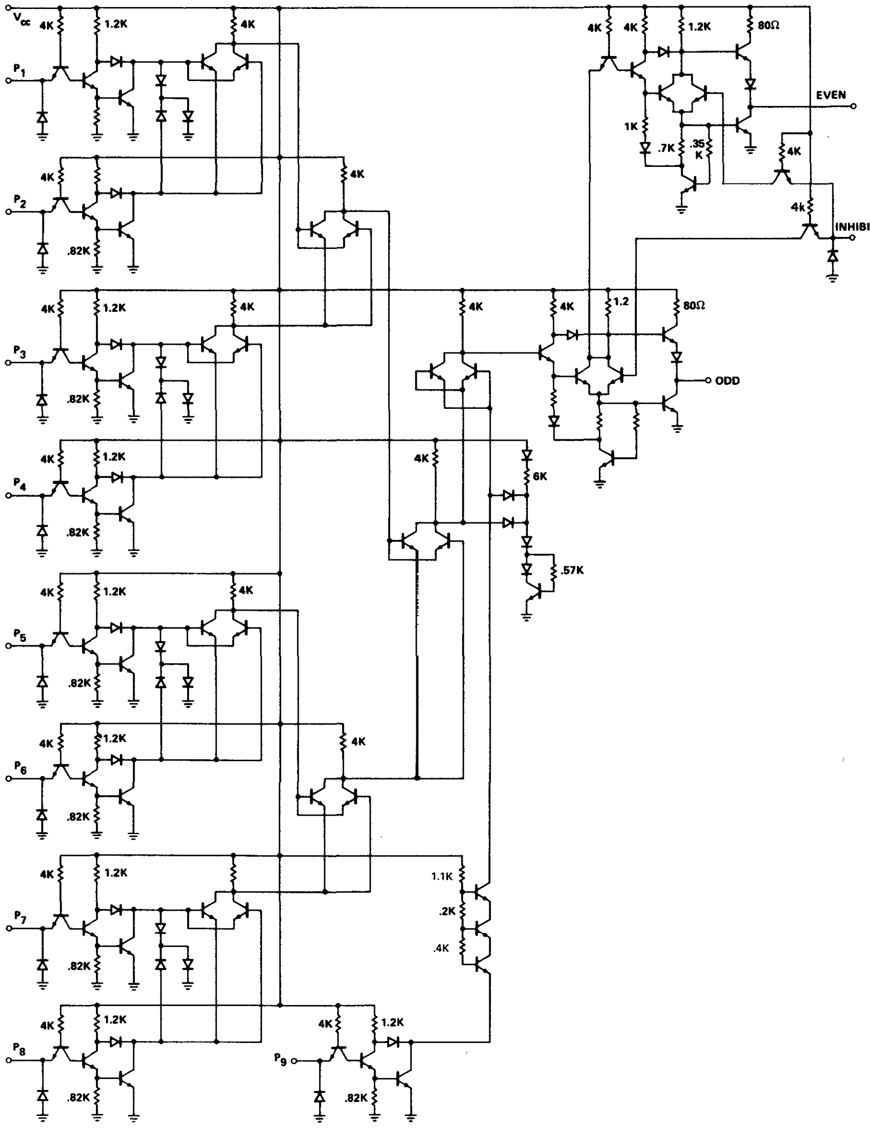
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN.	TYP.	MAX.	UNITS	UNDER TEST			
Turn-On Times								
P_1 - P_8 to Even		35	50	ns	Pulse			8
P_1 - P_8 to Odd		30	45	ns	Pulse			8
P_9 to Even		20	35	ns	Pulse			8
P_9 to Odd		15	30	ns	Pulse			8
Inhibit to Even		8	15	ns		Pulse		8
Inhibit to Odd		8	15	ns		Pulse		8
Turn-Off Times								
P_1 - P_8 to Even		38	55	ns	Pulse			8
P_1 - P_8 to Odd		32	45	ns	Pulse			8
P_9 to Even		23	40	ns	Pulse			8
P_9 to Odd		20	35	ns	Pulse			8
Inhibit to Even		10	18	ns		Pulse		8
Inhibit to Odd		10	18	ns		Pulse		8

NOTES:

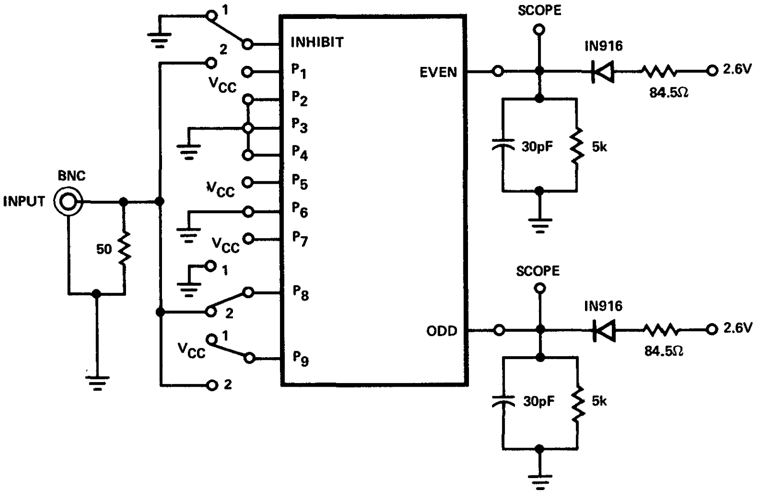
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic : "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
11. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM

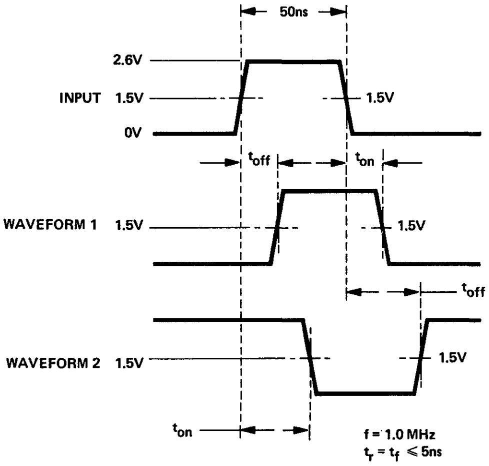


AC TEST FIGURE AND WAVEFORMS

8262 PARITY GENERATOR-CHECKER



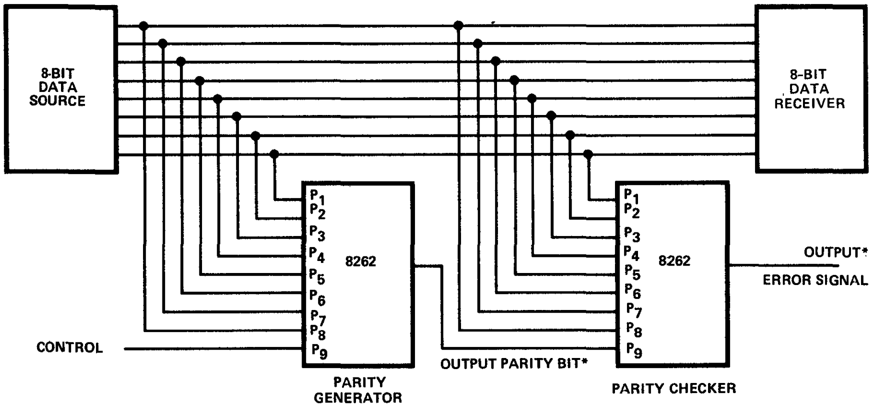
PULSE REQUIREMENTS



TRUTH TABLE

MEASURE DELAY FROM	SWITCH POSITION			WAVEFORM	
	INH	P_8	P_9	EVEN	ODD
P_8 to ODD	1	2	1		1
P_9 to ODD	1	1	2		2
P_8 to EVEN	1	2	1	2	
P_9 to EVEN	1	1	2	1	
INH to EVEN	2	1	1	2	

TYPICAL APPLICATIONS



*Output can be conditioned for odd or even parity.

An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.

An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

3-INPUT, 4-BIT DIGITAL

8263
8264

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.
The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus, eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

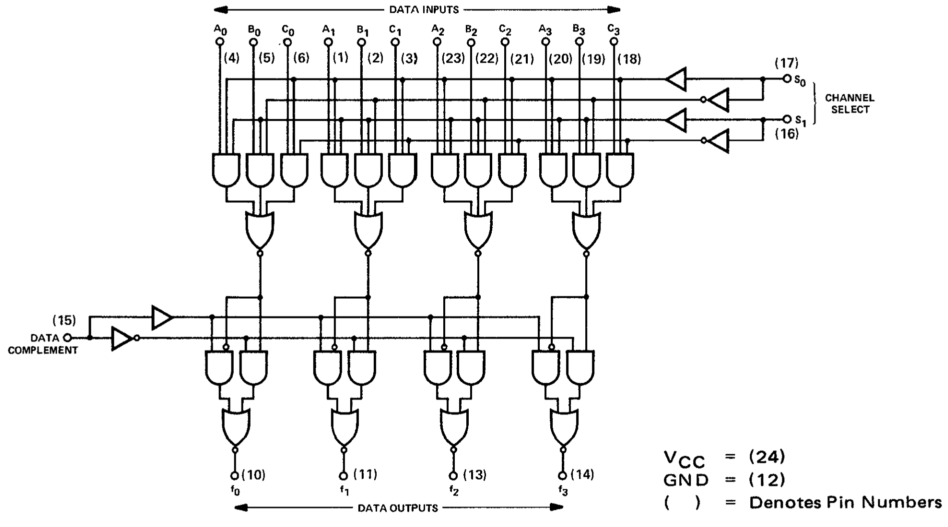
TRUTH TABLE

Data Input $A_n B_n C_n$	Channel Select S_0 S_1	Data Complement	Output Enable (8264)	Data Outputs
A_n x x	1 1	0	1	A_n
x B_n x	0 1	0	1	B_n
x x C_n	1 0	0	1	C_n
x x x	0 0	0	1	0
A_n x x	1 1	1	1	$\overline{A}_n$
x B_n x	0 1	1	1	$\overline{B}_n$
x x C_n	1 0	1	1	$\overline{C}_n$
x x x	0 0	1	1	1
x x x	x x	x	0	1

X = Either State

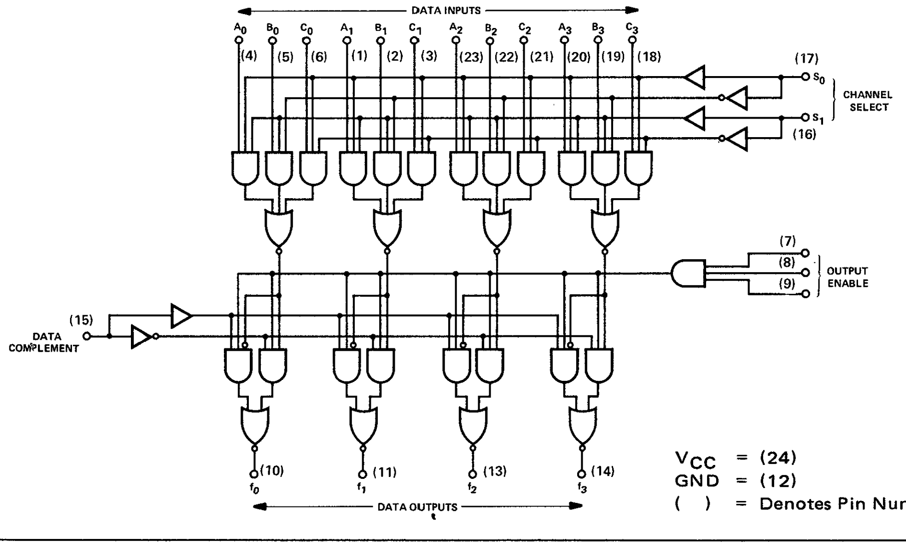
LOGIC DIAGRAMS

8263



V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8264



V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	C_n	S_0	S_1	DATA COMP	OUTPUT ENABLE	OUTPUTS	
"1" Output Voltage (8263)	2.6	3.5		V	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V		800µA	8
"1" Output Leakage Current (8264)			200	µA	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V	2.0V		11
"0" Output Voltage (8263)			0.4	V	0.8V	0.8V	0.8V	2.0V	2.0V	0.8V		9.6mA	9
"0" Output Voltage (8264)			0.4	V	0.8V							16.0mA	11
"0" Input Current													
A_n	-0.1		-1.6	mA	0.4V								
B_n	-0.1		-1.6	mA		0.4V		0.4V					
C_n	-0.1		-1.6	mA			0.4V		0.4V				
OE, DC	-0.1		-1.6	mA						0.4V	0.4V		6
S_0, S_1	-0.1		-3.2	mA				0.4V	0.4V				
"1" Input Current													
A_n			40	µA	4.5V			0V	0V				
B_n			40	µA		4.5V			0V				
C_n			40	µA			4.5V	0V					
OE, DC			40	µA						4.5V	4.5V		
S_0, S_1			40	µA				4.5V	4.5V				

$T_A = 25°C$ and $V_{CC} = 5.0V$

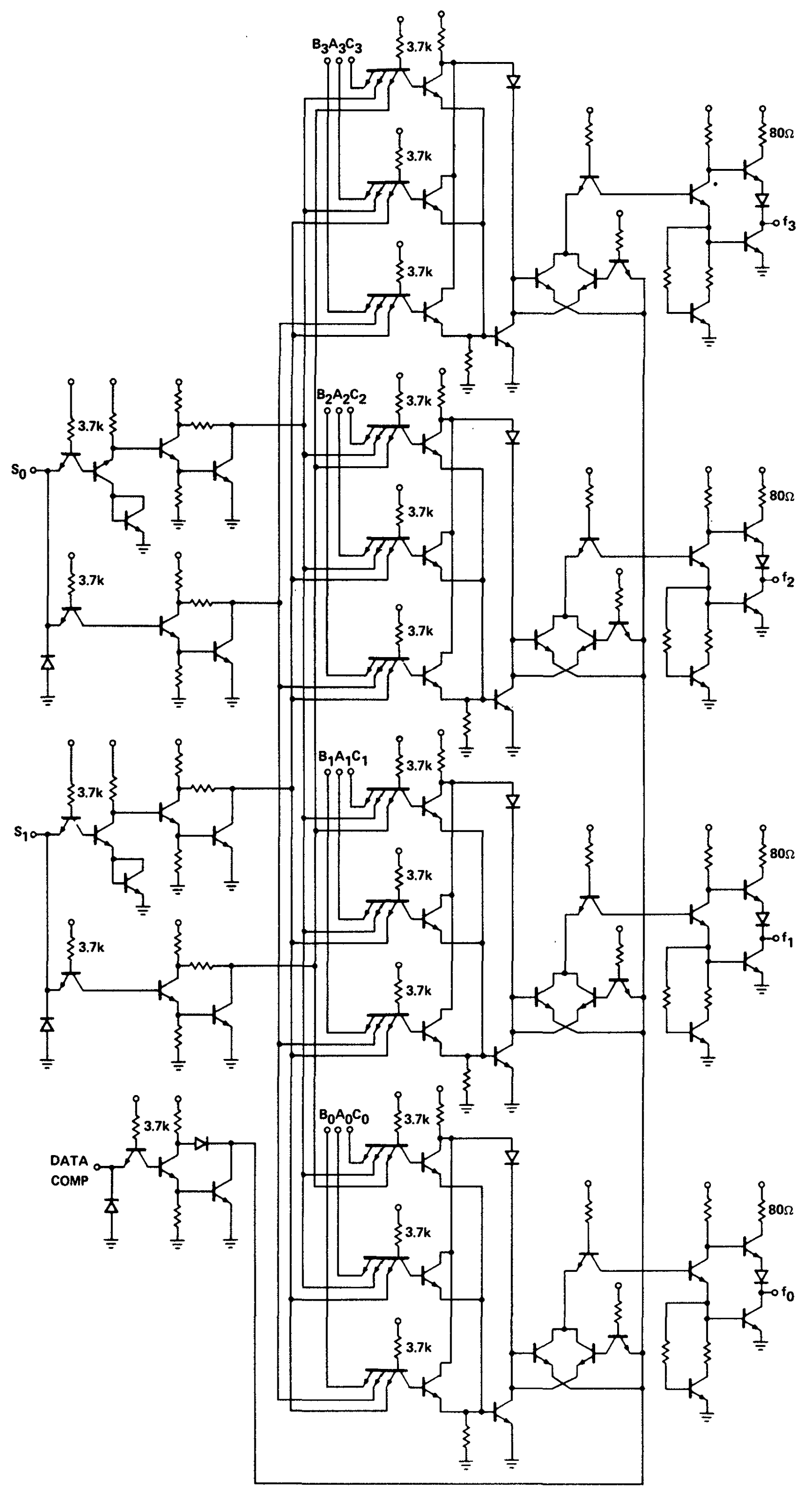
CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	C_n	S_0	S_1	DATA COMP	OUTPUT ENABLE	OUTPUTS	
Propagation Delay (8263)													
A_n to f_n		17	26	ns									10
S_0, S_1 to f_n		25	36	ns									10
DC to f_n		17	26	ns									10
Propagation Delay (8264)													
A_n to f_n		25	36	ns									10
S_0, S_1 to f_n		25	36	ns									10
DC to f_n		20	30	ns									10
OE to f_n		20	30	ns									10
Input Latch Voltage Rating													
A_n	5.5			V	10mA			0V	0V				12
B_n	5.5			V		10mA			0V				12
C_n	5.5			V			10mA	0V					12
S_0	5.5			V				10mA					12
S_1	5.5			V					10mA				12
DC	5.5			V						10mA			12
OE	5.5			V							10mA		12
Output Short Circuit Current	-20		-70									0V	
Power/Current Consumption													14
(8263)		378/	420/	mW/				0V					
		72	80	mA									
(8264)		400/	475/	mW/				0V					
		76	90.4	mA									

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electric Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25m Vrms. All pins not specifically referenced are tied to ground for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Refer to AC Test Figure.
11. Connect an external 1k ± 1% resistor from V_{CC} to the output for this test.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. *Manufacturer reserves the right to make design and process changes and improvements.*
14. V_{CC} = 5.25 volts.

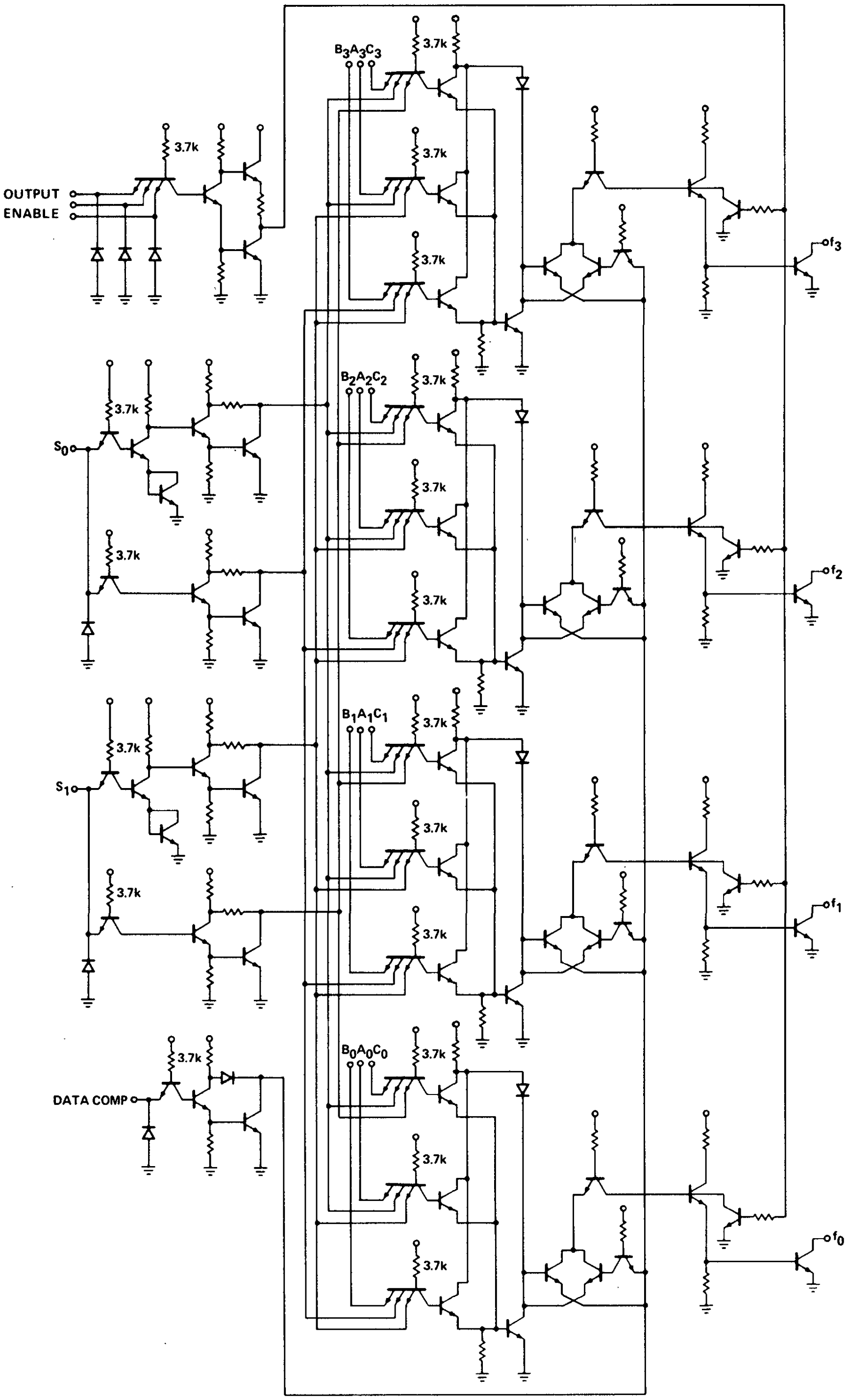
SCHEMATIC DIAGRAMS

8263



SCHEMATIC DIAGRAMS (Cont'd)

8264



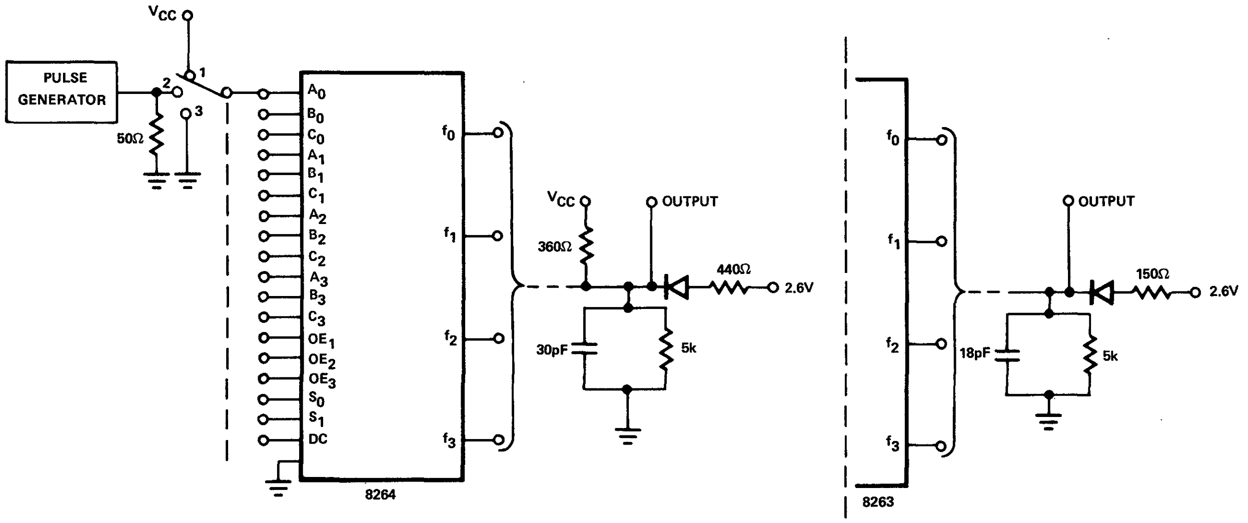
AC TESTING

Step No.	Delay From-To	Switching Positions																		Waveform Types
		Driven Inputs	Other Inputs																	
			A_0	B_0	C_0	A_1	B_1	C_1	A_2	B_2	C_2	A_3	B_3	C_3	OE	OE	OE	S_0	S_1	DC	
1	A_n to f_n	2	2	1	1	2	1	1	2	1	1	2	1	1	1	1	1	1	1	1	C, D
2	S_0 to f_n	2	3	1	1	3	1	1	3	1	1	3	1	1	1	1	1	2	1	1	A, B
3	S_0 to f_n	2	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	1	C, D
4	S_1 to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	C, D
5	DC to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	C, D
6	OE_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	*	*	*	1	1	1	C, D

NOTE: Step number 6 is for 8264 only.

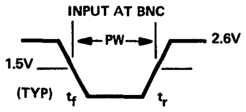
* Test one input at a time - others remain at "1".

AC TEST FIGURE AND WAVEFORMS



NOTE:
1. Scope terminals to be < 1½" from package pins.
2. Position 1 on switch provides a logical "1". Position 2 on switch provides pulse. Position 3 on switch provides a logical "0".
3. All measurements are made at 1.5V level.
4. See truth table for logical conditions.

NON-INVERTING PATHS



$t_r = t_f \leq 3ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz

INVERTING PATHS

TYPICAL APPLICATIONS

An approach to expanding the 8264 (bare collector output) is shown in Figure 1. The idea is to use common collectors with external pull-up resistors (one resistor for each of the four outputs) and make use of the output enable code.

As can be seen, the channel select lines are tied common, while a different enable code would be used to select a particular 8264. All non-selected 8264's have their outputs in the logic "1" condition, thus allowing the selected multiplexer to predominate.

Figure 2 illustrates a typical example using the 8263 (totem pole output) along with the 8281 (4-bit binary counter) and the 8270/71 (4-bit shift register), to implement a variable modulus counter. The 8270's act as a 3-register memory. The outputs of the 8270's are fed to the corresponding inputs of the 8263. Now there are three different presettable 4-bit words that can be chosen by the 8264. By alternating the channel select codes, the 8281 counter is preset with one of three words and produces an output whose repetition rate is dependent on the inputs from the multiplexer.

EXPANDING THE 8264

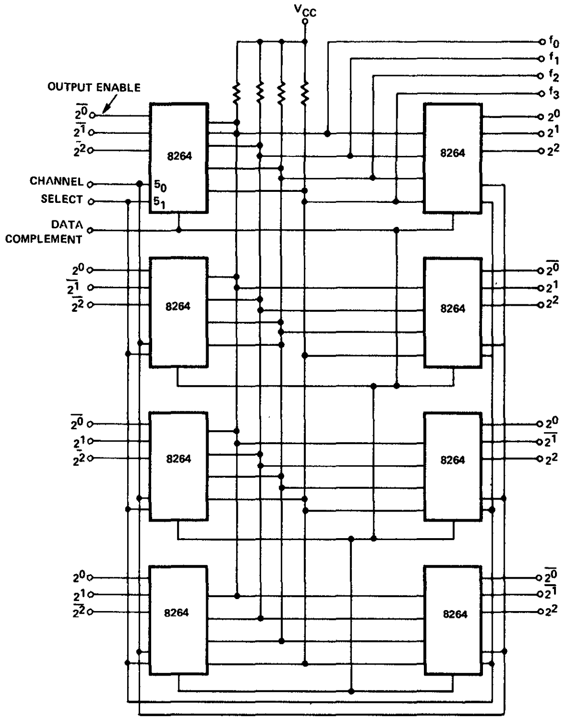


FIGURE 1

VARIABLE MODULUS COUNTER

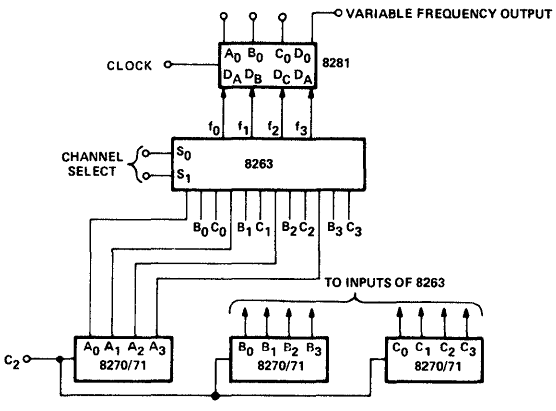


FIGURE 2

2-INPUT, 4-BIT DIGITAL MULTIPLEXER

8266 8267

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

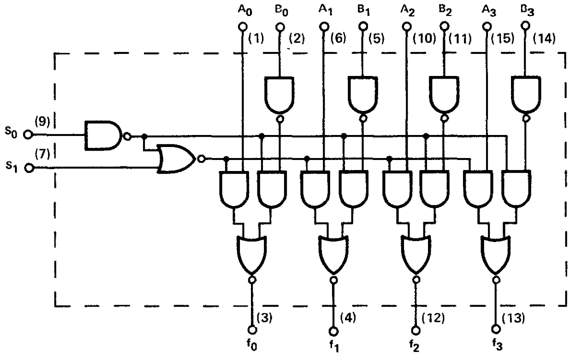
The 8266/8267 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing familiar TTL circuit structures. The 8267 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3), B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

LOGIC DIAGRAM

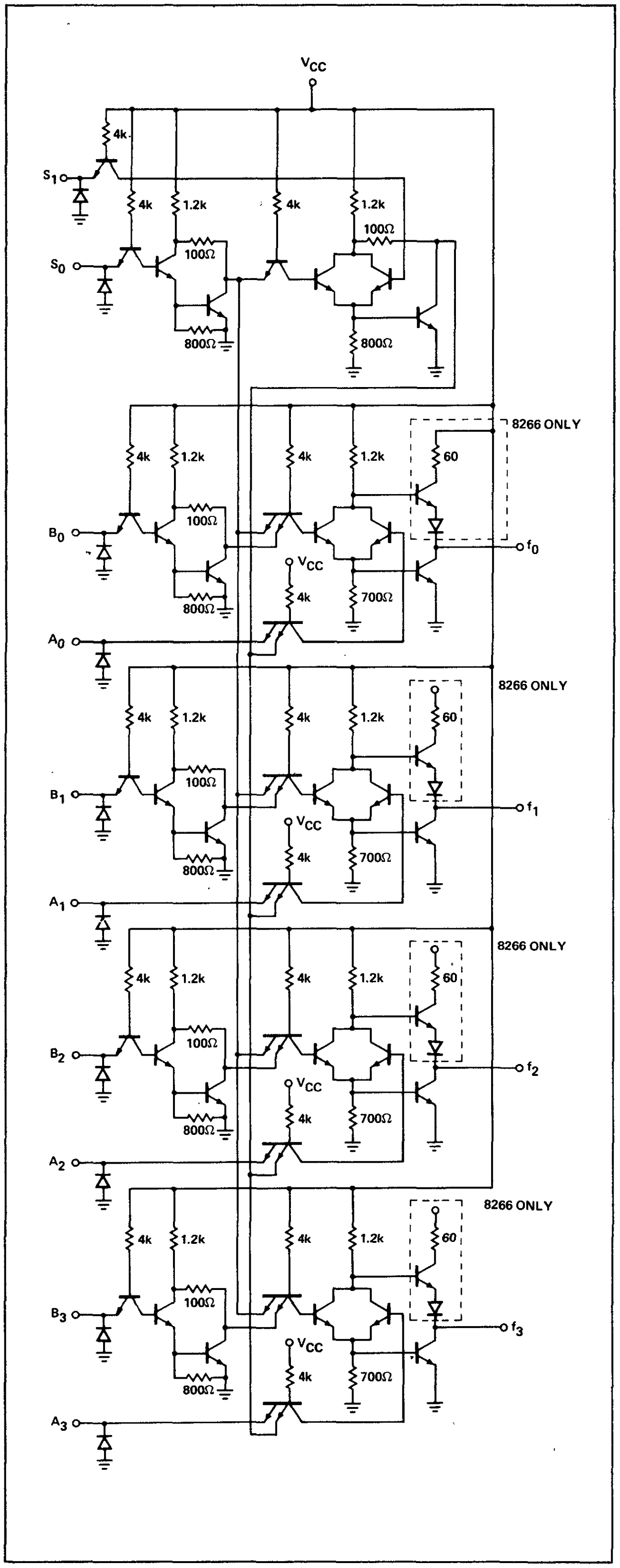


V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

TRUTH TABLE

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\bar{A}_n$
1	1	1

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
"1" Output Voltage (8266)	2.6	3.5		V	0.8V	2.0V	0.8V	0.8V	-800μA	7
"0" Output Voltage			0.40	V	2.0V	2.0V	2.0V	0.8V	16mA	8
"1" Output Leakage Current (8267)			25	μA	0.6V	2.0V	2.0V	0.8V		10
"0" Input Current										
A_n, B_n	-0.1		-1.6	mA	0.4V	0.4V	0V	0V		
S_0, S_1	-0.1		-1.6	mA			0.4V	0.4V		
"1" Input Current										
A_n, B_n			40	μA	4.5V	4.5V		2.0V		
S_0, S_1			40	μA			4.5V	4.5V		
Input Voltage Rating										
S_0, A_n, B_n	5.5			V	10mA	10mA	10mA	2.0V		11
S_1	5.5			V			2.0V	10mA		11
Output Short Circuit Current (8266)	-20		-70	mA					0V	

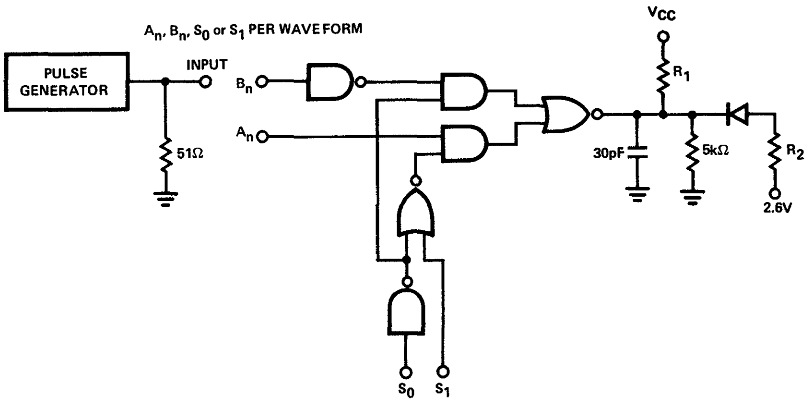
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
Propagation Delay (8266)										
S_0 to f_n (short path)		18	28	ns						9
S_0 to f_n (long path)		20	30	ns						9
A_n to f_n		13	20	ns						9
B_n, S_1 to f_n		14	25	ns						9
Propagation Delay (8267)										
S_0 to f_n		27	36	ns						9
A_n to f_n		15	20	ns						9
B_n, S_1 to f_n		21	28	ns						9
S_0 to f_n (short path)		18	28	ns						9
Power/Current Consumption		200/ 38.1	275/ 52.4	mW/ mA	4.5V	0V	4.5V	0V		13

NOTES:

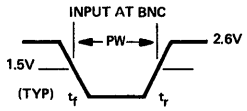
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. Connect an external 1k ±1% resistor from V_{CC} to the output for this test.
11. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. V_{CC} = 5.25 volts.

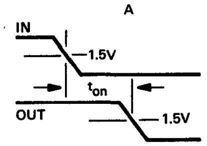
AC TEST FIGURE AND WAVEFORMS

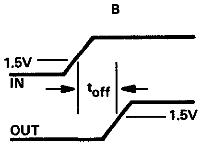


	8266	8267
R_1	∞	330Ω
R_2	84.5Ω	470Ω

NON-INVERTING PATHS

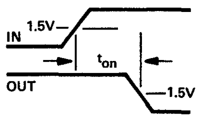


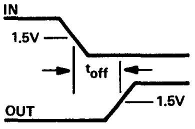




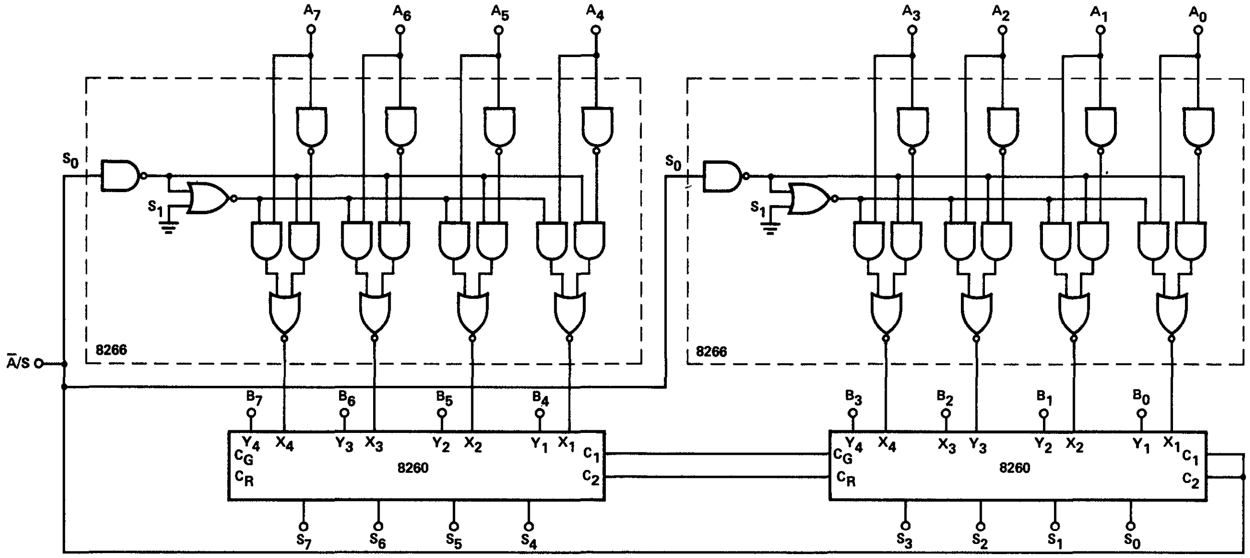
$t_r = t_f \leqslant 5ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz

INVERTING PATHS





TYPICAL APPLICATIONS



The 8266 can be used in conjunction with the 8260 (Look-Ahead Carry Adder) to form an adder-subtractor.

GATED FULL ADDER | 8268

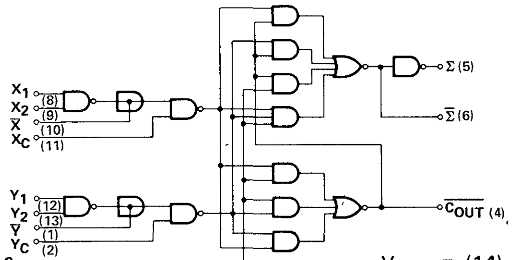
DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8268 is a single-bit full adder with gated true and complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and an inverted carry output. By taking advantage of the unique true or inverted inputs and true or inverted outputs, parallel addition speed is greatly enhanced (by eliminating unnecessary inversions).

The device is designed for medium speed parallel and serial adder systems.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

TRUTH TABLE (See Notes 1, 2 and 3)

C_{IN}	Y	X	$\overline{C_{OUT}}$	Σ	$\overline{\Sigma}$
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES:

1. $X = \overline{\overline{X} \cdot X_c}$; $Y = \overline{\overline{Y} \cdot Y_c}$
   where $\overline{X} = \overline{X_1 \cdot Y_2}$; $\overline{Y} = \overline{Y_1 \cdot Y_2}$
2. When $\overline{X}$ or $\overline{Y}$ are used as inputs, X_1 and X_2 or Y_1 and Y_2 respectively must be tied to GND.
3. When X_1 and X_2 or Y_1 and Y_2 are used as inputs, $\overline{X}$ or $\overline{Y}$ respectively must be left open or used to perform the WIRED-AND function.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS										NOTES
	MIN.	TYP.	MAX.	UNITS	X_1	X_2	X	X_c	Y_1	Y_2	Y	Y_c	C_{IN}	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	0.8V	2.0V	2.0V	0.8V	0.8V	0.8V	2.0V	0.8V	-500μA	6
"0" Output Voltage			0.4	V	0.8V	0.8V	2.0V	2.0V	0.8V	0.8V	2.0V	2.0V	0.8V	16mA	7
"0" Input Current															
X_1	-0.1		-1.6	mA	0.4V	4.5V									
X_2	-0.1		-1.6	mA	4.5V	0.4V									
$\overline{X}$	-0.1		-2.6	mA	0.0V	0.0V	0.4V	4.5V							
X_c	-0.1		-1.6	mA	0.0V	0.0V		0.4V							
Y_1	-0.1		-1.6	mA					0.4V	4.5V					
Y_2	-0.1		-1.6	mA					4.5V	0.4V					
$\overline{Y}$	-0.1		-2.6	mA					0.0V	0.0V	0.4V	4.5V			
Y_c	-0.1		-1.6	mA					0.0V	0.0V		0.4V			
C_{IN}	-0.1		-8.0	mA									0.4V		
"1" Input Current															
X_1			40	μA	4.5V										
X_2			40	μA	0.0V										
X_c			40	μA			0.0V	4.5V							
Y_1			40	μA					4.5V	4.5V					
Y_2			40	μA					0.0V	0.4V					
Y_c			40	μA							0.0V	4.5V			
C_{IN}			160	μA	0.0V	0.0V			0.0V	0.0V			4.5V		
Input Voltage Rating															12
X_1	5.5			V	10mA	0.0V									
X_2	5.5			V	0.0V	10mA									
X_c	5.5			V			0.0V	10mA							
Y_1	5.5			V					10mA	0.0V					
Y_2	5.5			V					0.0V	10mA					
Y_c	5.5			V							0.0V	10mA			
C_{IN}	5.5			V									10mA		

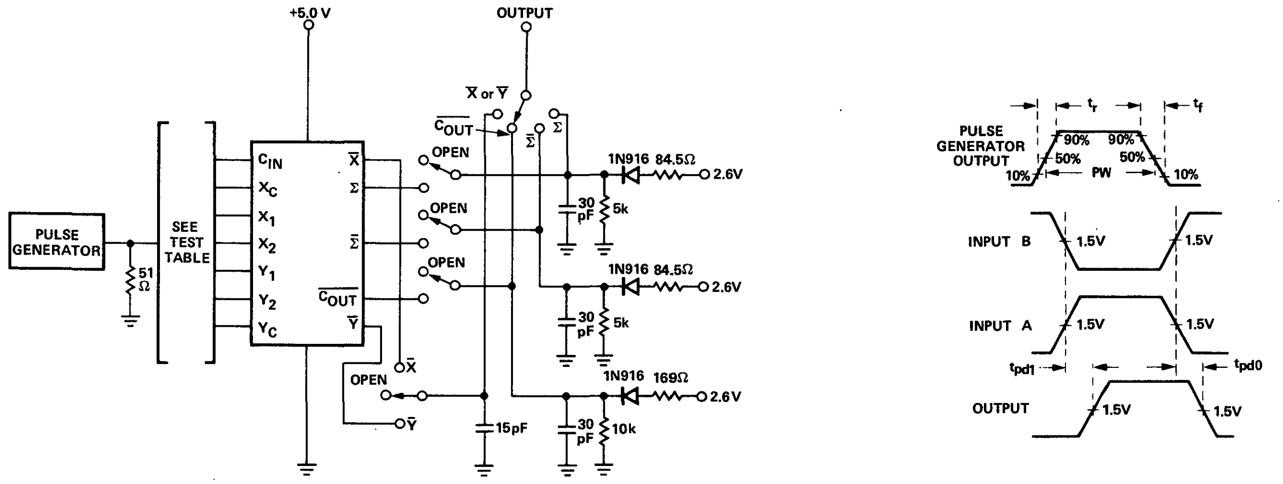
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS										NOTES
	MIN.	TYP.	MAX.	UNITS	X_1	X_2	X	X_c	Y_1	Y_2	Y	Y_c	C_{IN}	OUTPUTS	
Power/Current Consumption		152/ 29	185/ 35	mW/ mA											14
Output Short Circuit Current (Σ)	-18		-57	mA	0.0V	0.0V			0.0V	0.0V	0.0V		2.0V	0.0V	11, 14
Output Short Circuit Current ($\overline{\Sigma}$)	-18		-57	mA	0.0V	0.0V			0.0V	0.0V			0.0V	0.0V	11, 14
Output Short Circuit Current ($\overline{C}_{out}$)	-18		-70	mA	0.0V	0.0V			0.0V	0.0V			0.0V	0.0V	11, 14
t_{pd} 1 C_{in} to $\overline{C}_{out}$		8	13	ns											8
t_{pd} 0 C_{in} to $\overline{C}_{out}$		8	13	ns											8
t_{pd} 1 Y_c to $\overline{C}_{out}$		20	25	ns											8
t_{pd} 0 Y_c to $\overline{C}_{out}$		20	25	ns											8
t_{pd} 1 X_c to Σ		35	45	ns											8
t_{pd} 0 X_c to Σ		35	45	ns											8
t_{pd} 1 Y_c to $\overline{\Sigma}$		25	35	ns											8
t_{pd} 0 Y_c to $\overline{\Sigma}$		25	35	ns											8
t_{pd} X_1, X_2 to $\overline{X}$		30	40	ns											8, 9
t_{pd} 0 X_1, X_2, to $\overline{X}$		15	20	ns											8, 9
t_{pd} 1 Y_1, Y_2, to $\overline{Y}$		30	40	ns											8, 9
t_{pd} 0 Y_1, Y_2, to $\overline{Y}$		15	20	ns											8, 9

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}
8. Refer to AC Test Figure.
9. This test is a measure of the required worst-case data set-up time.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. Not more than one output should be shorted at a time.
12. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. The total time required to perform the ADD function may be determined by summing the delays from X_1, X_2 to $\overline{X}$ or Y, Y_2 to $\overline{Y}$ with the delay from X_C or Y_C to Σ or $\overline{\Sigma}$.
14. V_{CC} = 5.25 volts.

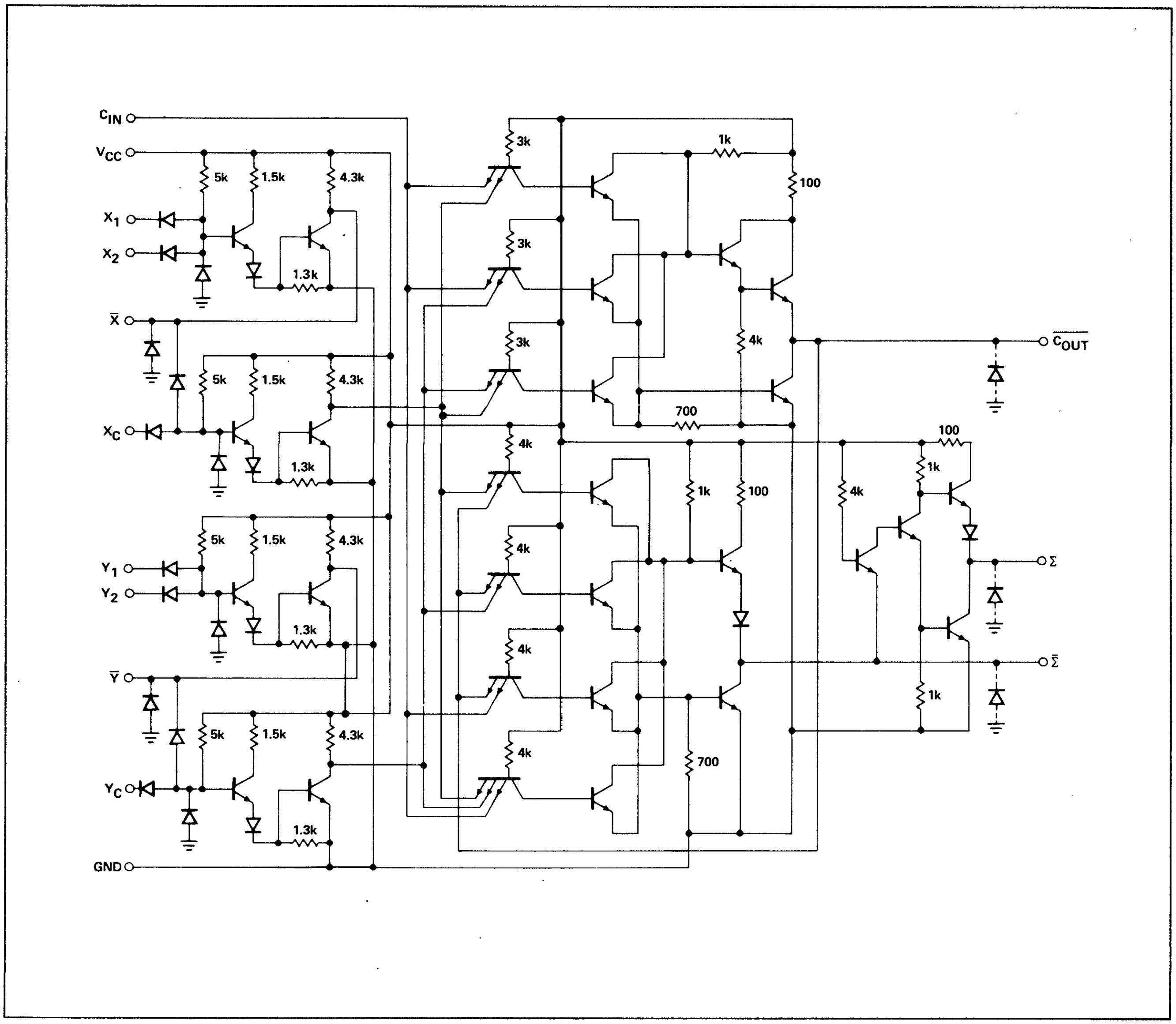
AC TEST FIGURE AND WAVE FORMS



NOTES:

1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 2.6V, tr = tf $\leqslant$ 15ns. PW = 0.5ns, PRR = 1MHz.
5. Inputs and outputs not otherwise specified are open.
6. Capacitance shown include probe and jig capacitance.
7. All resistances are in ohms.

SCHEMATIC DIAGRAM

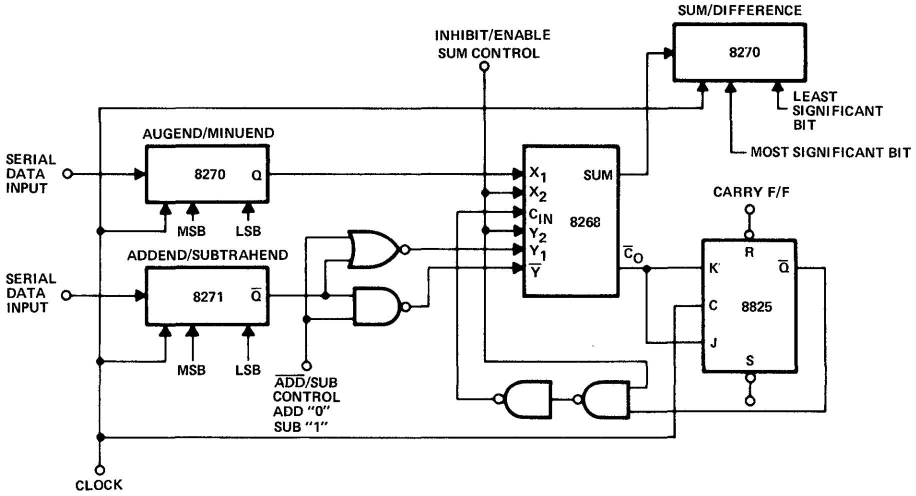


TEST TABLE (See Note 5)

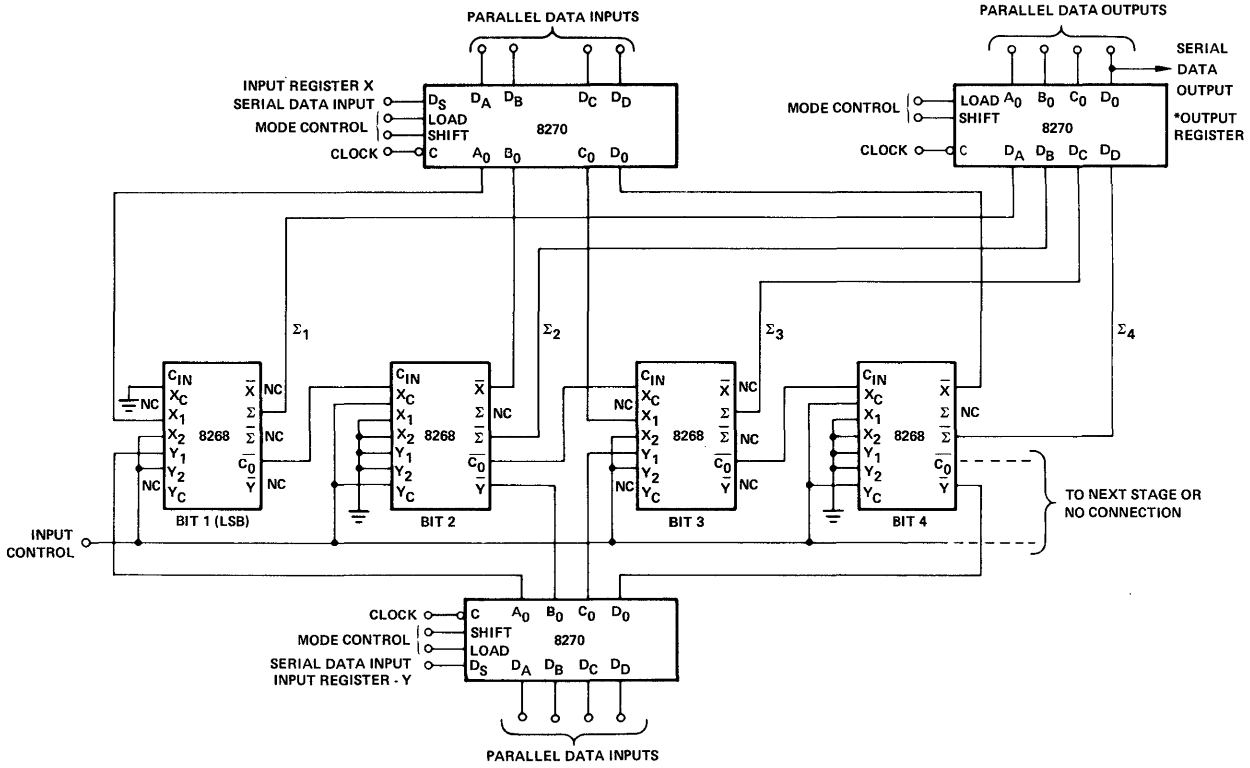
TEST NO.	OUTPUTS UNDER TEST	APPLY INPUT A TO	APPLY INPUT B TO	APPLY +2.6V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
2	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
3	$\overline{C}_{out}$	Y_c	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
4	$\overline{C}_{out}$	Y_c	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
5	Σ	X_c	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
6	Σ	X_c	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
7	$\overline{\Sigma}$	Y_c	None	C_{in}	Y_1	$\overline{\Sigma}$
8	$\overline{\Sigma}$	Y_c	None	C_{in}	Y_1	$\overline{\Sigma}$
9	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
10	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
11	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15 pF)
12	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15 pF)

TYPICAL APPLICATIONS

4-BIT SERIAL ADD/SUBTRACTOR



N-BIT PARALLEL ADDER



NOTES:

To expand storage register for serial/parallel operation, connect D_Q to D_s of next stage and common the mode control lines and the clock line of the first stage to their respective second stage equivalents.

*NOTE:

To expand output register for parallel outputs common clock, shift and load lines with their respective counterparts. For serial data output, also connect D_Q of first register to D_s of next register.

4-BIT COMPARATOR 8269

DIGITAL 8000 SERIES TTL/MSI

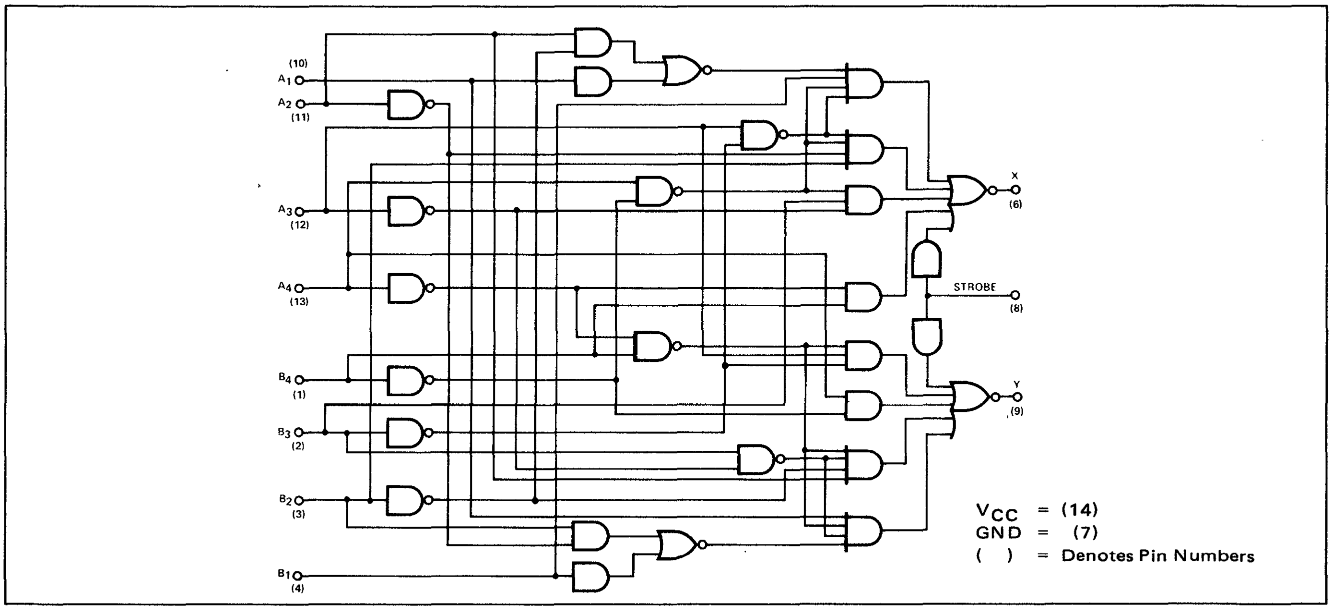
DESCRIPTION

The 8269, a 4 BIT COMPARATOR, is an array of gates designed to perform the numerical comparison of two four-bit binary numbers. The outputs indicate whether the two numbers are equal in value, or which number is the greater. The 8269 is a functional and pin-for-pin replacement for the DM8200.

TRUTH TABLE

INPUT				OUTPUT	
A_n		B_n	STROBE	X	Y
A	>	B	0	1	0
A	<	B	0	0	1
A	=	B	0	1	1
A	⋚	B	1	0	0

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
"1" Output Voltage	2.6	3.5		V	$I_{out} = 800\mu A$
"0" Output Voltage		0.2	0.4	V	$I_{out} = 16mA$
"1" Input Current			80	µA	$V_{in} = 4.5V$
"0" Input Current	-0.1		-3.2	mA	$V_{in} = 0.4V$
Power Consumption			278/53	mW/mA	$V_{CC} = 5.25V$
Short Circuit Output Current	- 18		-55	mA	$V_{out} = 0V$, $V_{CC} = 5.25V$
Input Latch Voltage	5.5			V	$I_{out} = 10mA$

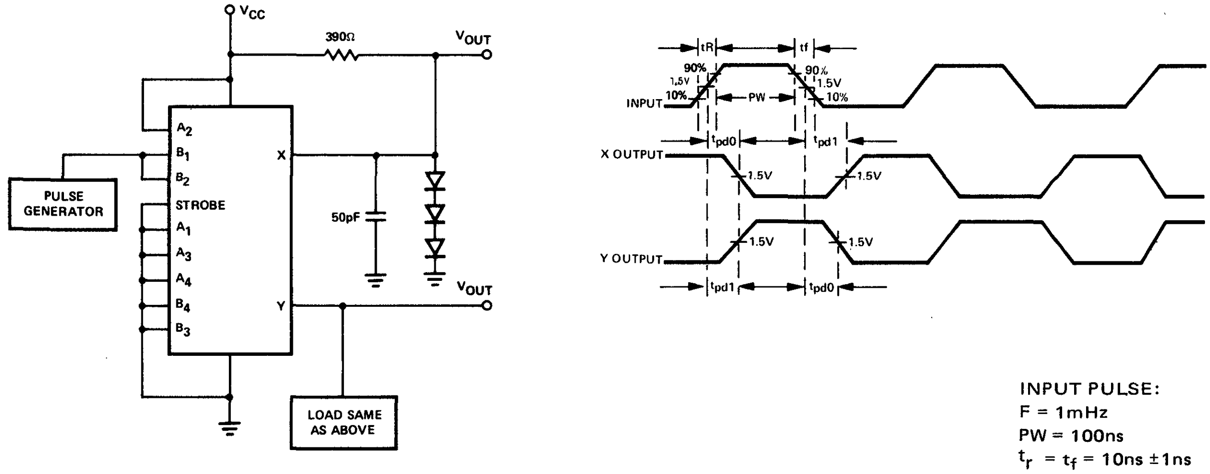
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Propagation Delay					
tpd1 (Data Input to Output)			40	ns	Test Figure 1
tpd0 (Data Input to Output)			30	ns	Test Figure 1
tpd1 (Strobe to Output)			27	ns	Test Figure 2
tpd0 (Strobe to Output)			18	ns	Test Figure 2

NOTES:

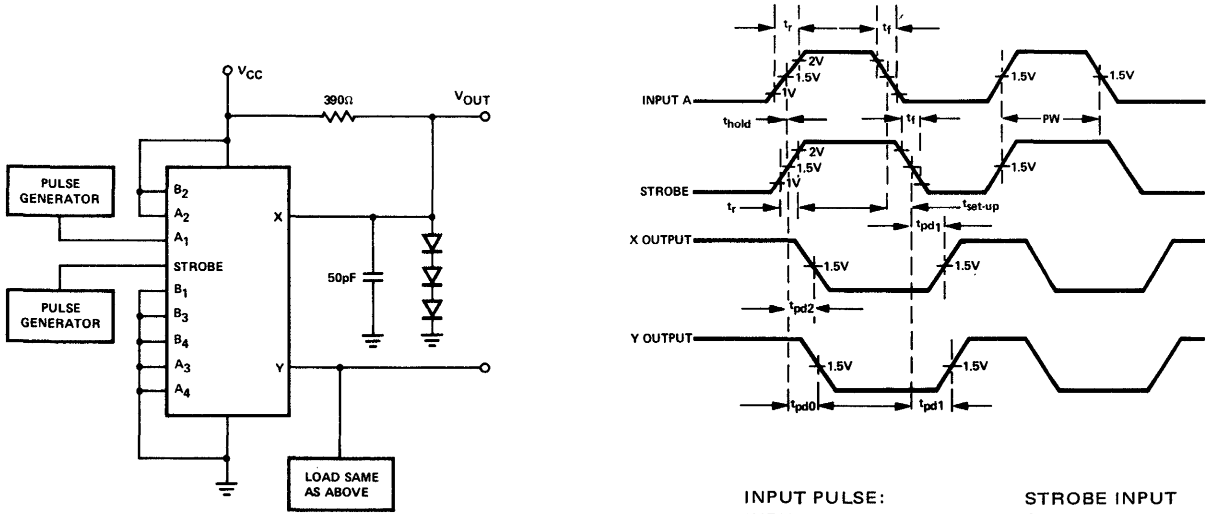
1. All voltage and capacitance measurements are referenced to the ground terminal.
   Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Manufacturer reserves the right to make design and process changes and improvements.

AC TEST FIGURE AND WAVEFORMS



INPUT PULSE:
F = 1mHz
PW = 100ns
t_r = t_f = 10ns ±1ns
AMP. = 3.0V

FIGURE 1



INPUT PULSE:
INPUT A
F = 1mHz
PW = 100ns
t_r = t_f = 10ns ±1ns
AMP. = 3.0V

STROBE INPUT
f = 1mHz
t_{hold} = 0ns
t_{set-up} = 10ns
t_r = t_f = 10ns ±1ns

FIGURE 2

4-BIT SHIFT REGISTERS 8270 8271

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8270 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver has been included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control.

The truth table for the control modes is shown below.

For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

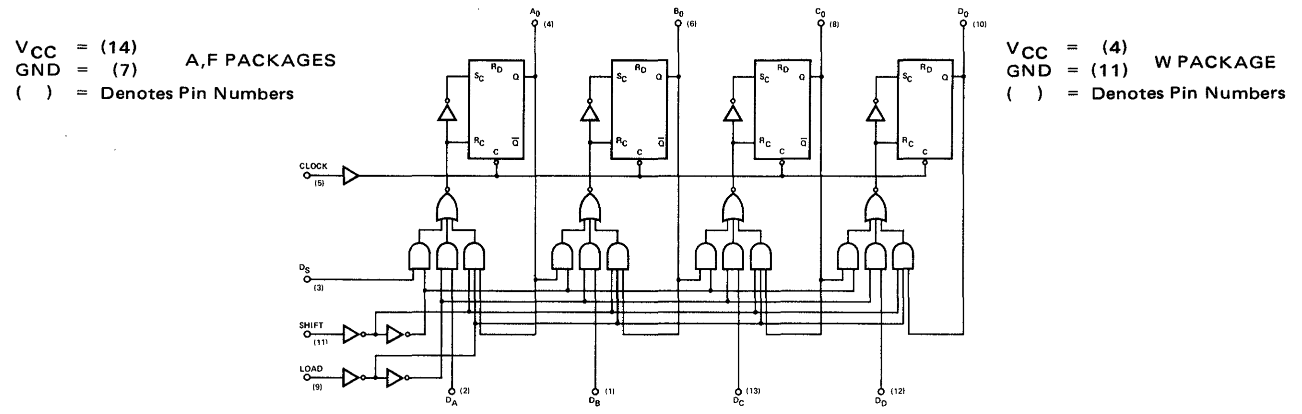
The 8271 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 8270 element. The fan-out specification for this output is the same as the true outputs of the 8270 element.

TRUTH TABLE

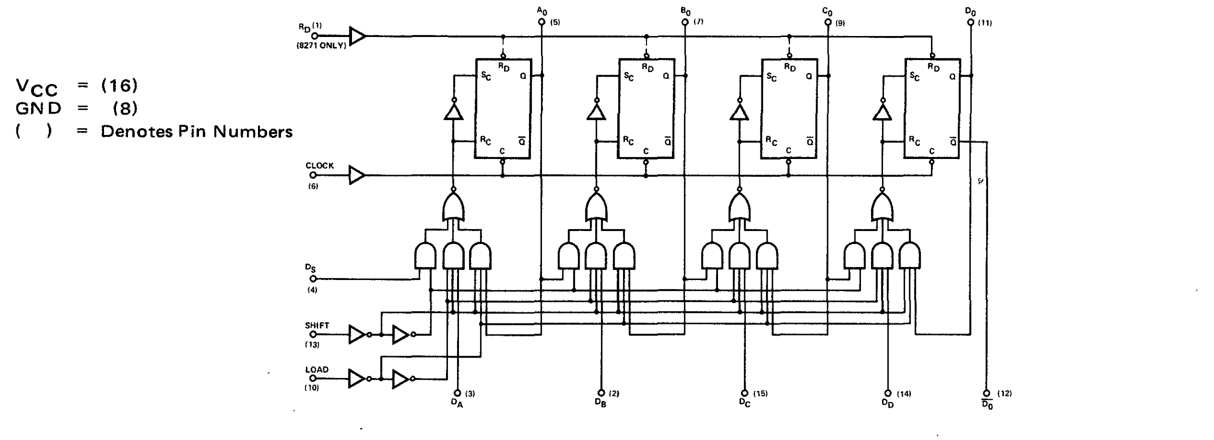
CONTROL STATE	LOAD	SHIFT
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

LOGIC DIAGRAM

(8270)



(8271)



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	LOAD	SHIFT	DATA INPUT	CLOCK	RESET 8271	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	0.8V	2.0V	Pulse	2.0V	-800μA	6
"0" Output Voltage			0.4	V	2.0V	0.8V	0.8V	Pulse	2.0V	11.2mA	7
"0" Input Current											
Load	-0.1		-1.2	mA	0.4V						
Shift	-0.1		-1.2	mA		0.4V	0.4V				
Data Input	-0.1		-1.2	mA			0.4V				
Clock	-0.1		-1.2	mA				0.4V			
Reset (8271 only)	-0.1		-1.2	mA					0V		
"1" Input Current											
Load			40	μA	4.5V						
Shift			40	μA		4.5V					
Data Input			40	μA			4.5V				
Clock			40	μA				4.5V			
Reset (8271 only)			40	μA					4.5V		
Input Voltage Rating											
(All Inputs)	5.5			V	10mA	10mA	10mA	10mA	10mA		

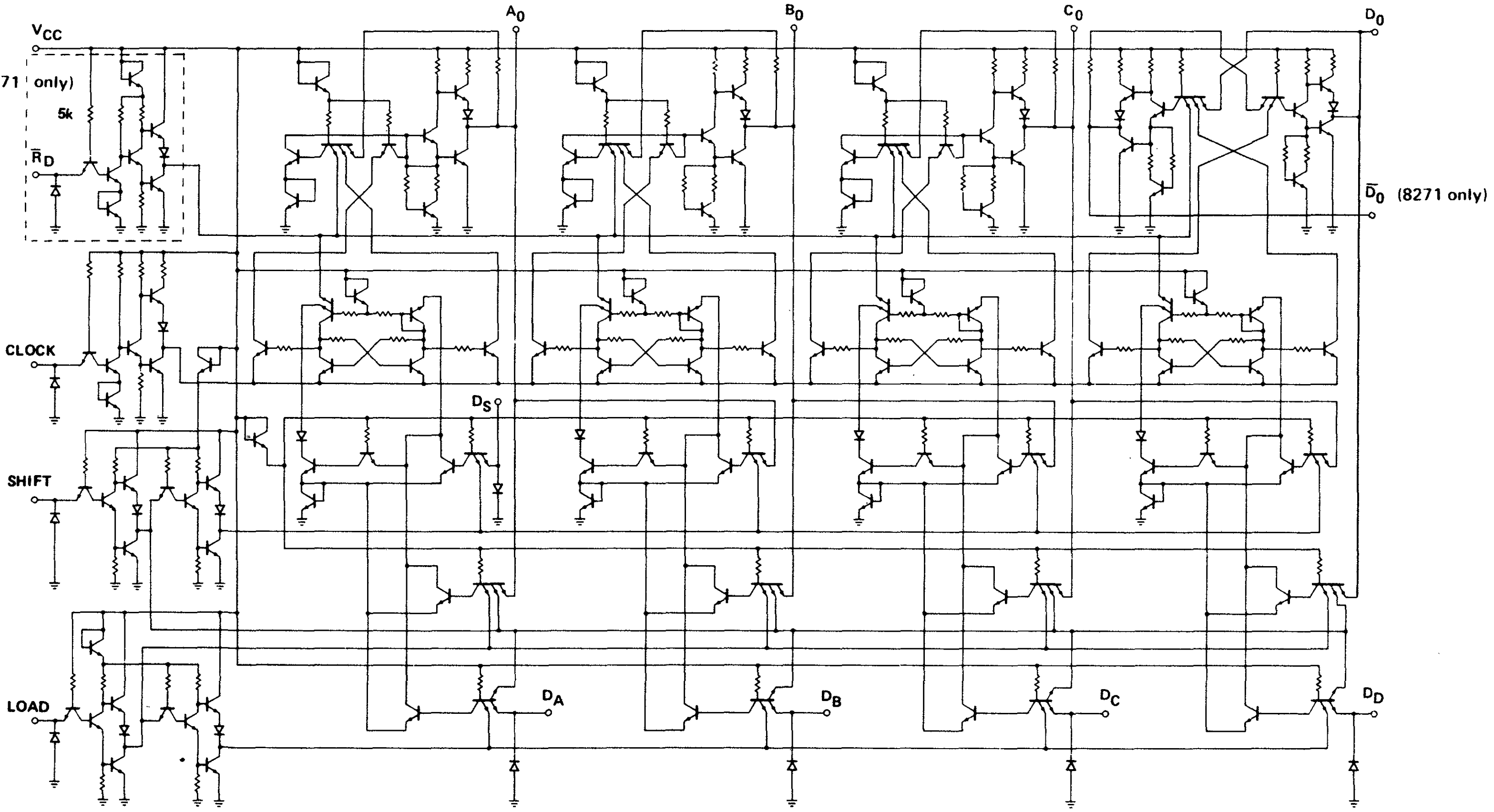
T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	LOAD	SHIFT	DATA INPUT	CLOCK	RESET 8271	OUTPUTS	
Power/Current Consumption											
8270 Only		168/32	247/47	mW/mA							10
8271 Only		271/52	344/65	mW/mA							10
Turn-On Delay											
All Binaries		25	40	ns							8
Turn-Off Delay											
All Binaries		25	40	ns							8
Clock "1" Interval	20			ns				2.0V			
Transfer Rate	15	22		MHz							
Shift Load Set-Up Time		20	30	ns							
Data Set-Up Time		7	15	ns							

NOTES:

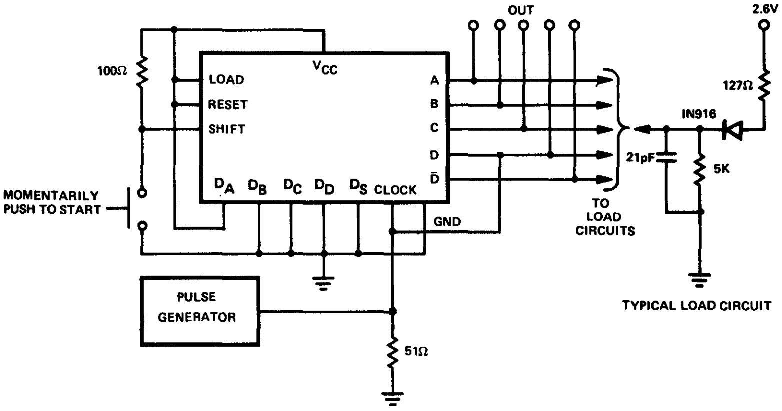
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Rating should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM



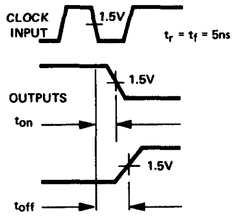
AC TEST FIGURES AND WAVEFORMS

TURN ON/OFF AND TRANSFER RATE



NOTES:

1. t_{on}/t_{off}



2. Transfer rate & min clock "1" level: check that binary outputs are changing.

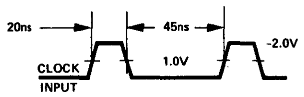
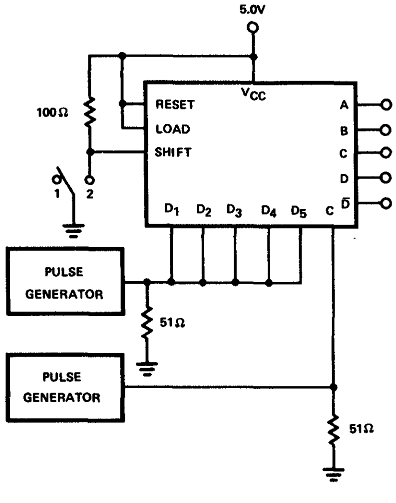
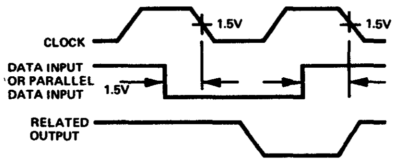


FIGURE 1

DATA SET-UP TIME



Load see Figure 1 above.



NOTES:

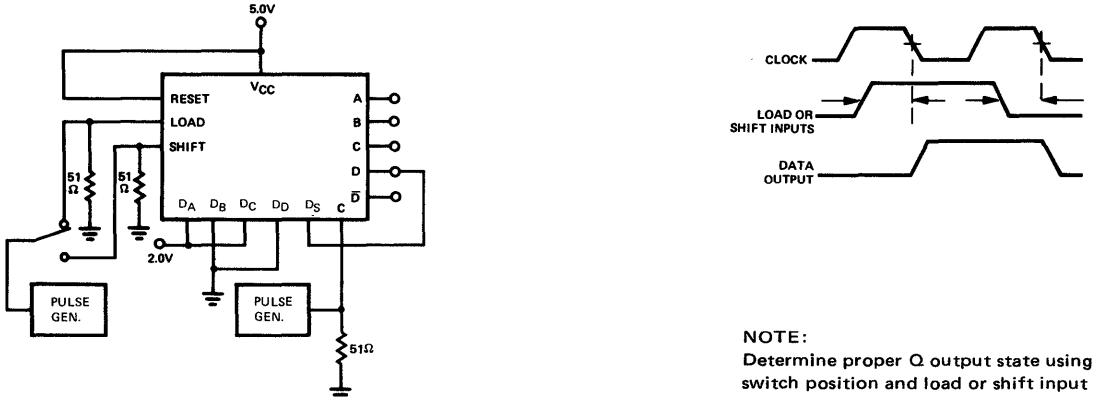
1. Switch in position 1 to test serial data input.
2. Switch in position 2 to test parallel data input.

Adjust data input or parallel input delays to test condition and verify output operation.

FIGURE 2

AC TEST FIGURES AND WAVEFORMS (Cont'd)

SHIFT/LOAD SET-UP TIME



NOTE:
Determine proper Q output state using switch position and load or shift input state before clocking transition.

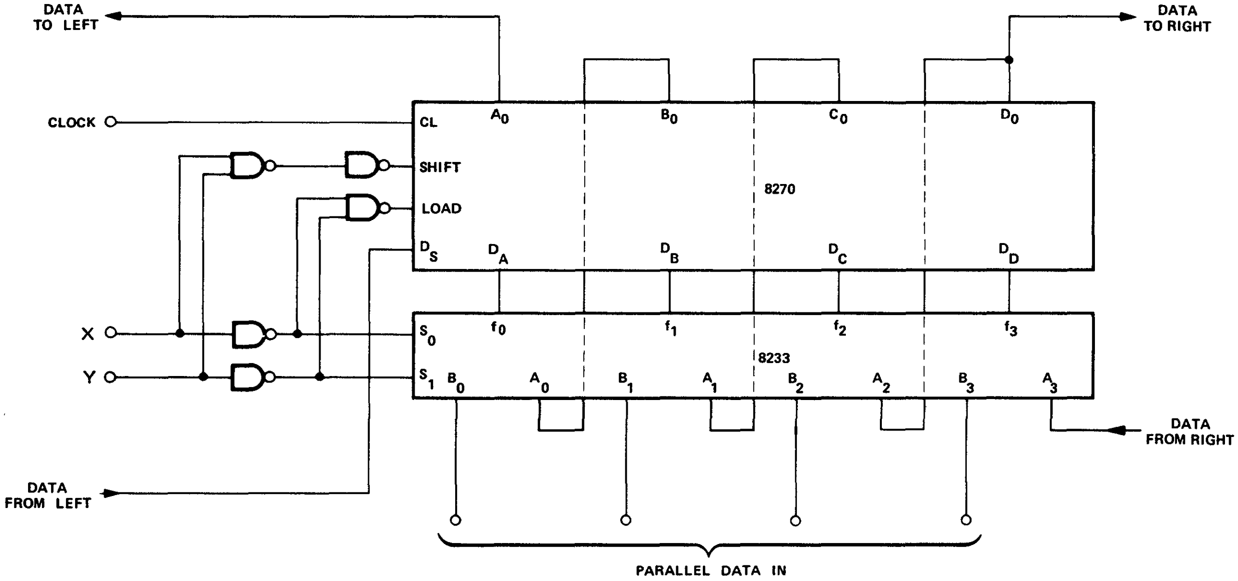
FIGURE 3

NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{AC} = mV rms.
3. All diodes are 1N916.

TYPICAL APPLICATIONS

SHIFT-RIGHT/SHIFT-LEFT/PARALLEL ENTRY SHIFT REGISTER



X	Y	Function
0	0	Hold
0	1	Shift Left
1	0	Parallel Load
1	1	Shift Right

Package Count: 1-8270
1-8233
½-8H90
½-8H80

10-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

8273

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

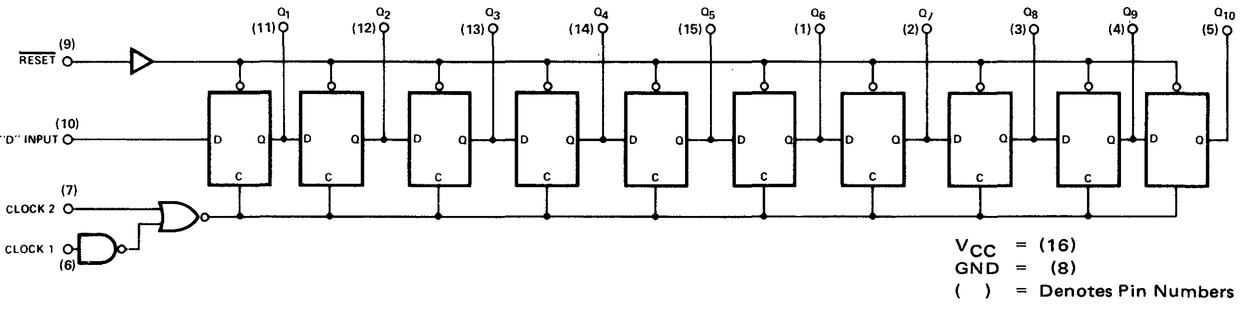
The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

TRUTH TABLE

INPUT	$\overline{\text{RESET}}$	CLOCK 1	CLOCK 2	$Q_n + 1$
1	1	Pulse	0	1
0	1	Pulse	0	0
1	1	1	Pulse	1
0	1	1	Pulse	0
1	1	Pulse	1	Q
0	1	Pulse	1	Q
1	1	0	Pulse	Q
0	1	0	Pulse	Q

NOTE: The unused clock input performs the INHIBIT function.
$\overline{\text{RESET}} = 0 \Rightarrow Q = 0$

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS	"D" INPUT	CLOCK 1	CLOCK 2	RESET		
"1" Output Voltage	2.6	3.4		V	2.0V	Pulse	0.8V		-500µA	6
"0" Output Voltage		0.2	0.4	V	0.8V	Pulse	0.8V		9.6mA	7
"0" Input Current										
"D" Input	-0.1		-1.6	mA	0.4V					
Clock 1	-0.1		-1.6	mA		0.4V				
Clock 2	-0.1		-1.6	mA			0.4V			
Reset	-0.1		-1.6	mA				0.4V		
"1" Input Current										
"D" Input			40	µA	4.5V					
Clock 1			40	µA		4.5V				
Clock 2			40	µA			4.5V			
Reset			40	µA				4.5V		
Input Voltage Rating (All Inputs)	5.5			V	10mA	10mA	10mA	10mA		

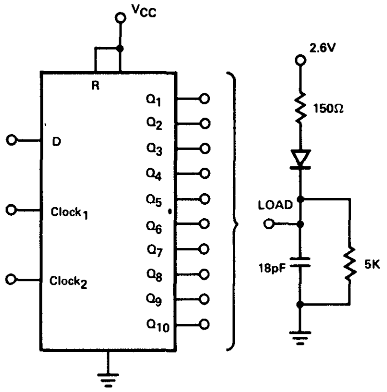
$T_A = 25°C$ and $V_{CC} = 5.0V$

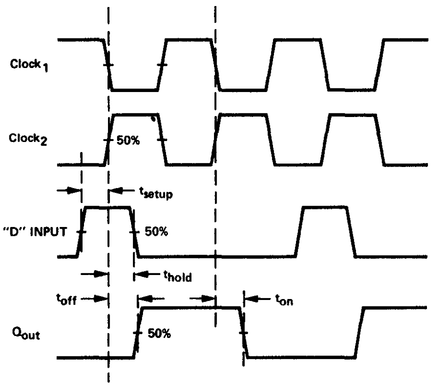
CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS	"D" INPUT	CLOCK 1	CLOCK 2	RESET		
Max. Data Transfer Rate	25	35		MHz						
Turn-On Delay										
Clock 1 to Output		32	40	ns			0.0V	4.5V		
Clock 2 to Output		28	40	ns				4.5V		
Reset to Output		35	50	ns		4.5V				
Turn-Off Delay										
Clock 1 to Output		25	40	ns			0.0V			
Clock 2 to Output		19	40	ns		4.5V				
Clock Pulse Width										
Clock 1		16	25	ns			0.0V			
Clock 2		12	20	ns		4.5V				
Set-Up Time (t_{set-up})										
Clock 1			15	ns			0.0V			
Clock 2			10	ns		4.5V				
Hold Time (t_{hold})										
Clock 1			15	ns			0.0V			
Clock 2			10	ns		4.5V				
Power Consumption			540	mW						8
Short Circuit Output Current	-20		-70	mA						
Input Voltage Rating (All Inputs)	5.5			V	10mA	10mA	10mA	10mA		

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. $V_{CC} = 5.25V$.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. See AC Test Figure.

AC TEST FIGURE AND WAVEFORMS





NOTES:

1. Unused clock 2 input must be grounded.
2. Input pulse characteristics
   CLOCK
   Amplitude = 3.0V
   $t_r = t_f \leqslant 5ns$.

10-BIT PARALLEL-IN, SERIAL-OUT SHIFT REGISTER

8274

DIGITAL 8000 SERIES TTL/MSI

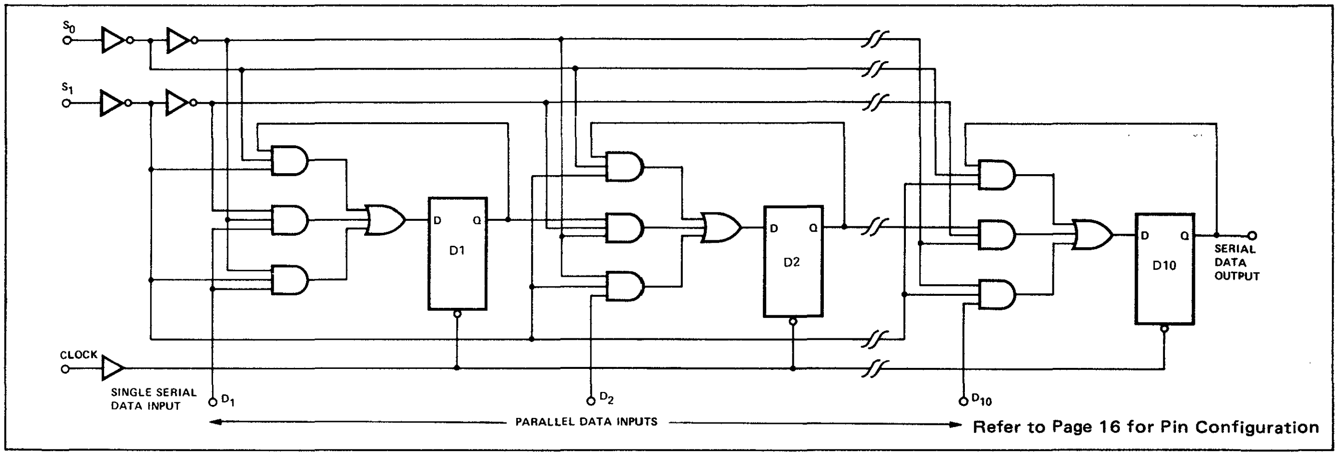
DESCRIPTION

The 8274 10-Bit Shift Register is an array of binary elements interconnected to perform the parallel-in, serial-out shift function. The circuit has ten parallel inputs and a single true serial output. The D_1 input can also be used for serial entry. Two control inputs, S_0 and S_1, determine the operating mode of the shift register as shown in the Truth Table. A single buffered clock line connects all ten flip-flops which are activated on the high-to-low transition of the clock pulse. Guaranteed input clock frequency is 25MHz. With the exception of the Hold Mode, the control inputs may be changed when the clock is in either the high or low state without causing false triggering. The Hold Mode can be entered only when the clock is low. Applications for the 8274 Shift Register include Parallel-to-Serial conversion, Modem Data Transmission, Pseudo-Random Code generation and Modulo-N Frequency Division.

TRUTH TABLE

S_0	S_1	OPERATING MODE
0	0	Hold
0	1	Clear
1	0	Load
1	1	Shift

LOGIC DIAGRAM



Refer to Page 16 for Pin Configuration

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	S_0	S_1	CLOCK	OUTPUTS	
"1" Output Voltage	2.6	3.4		V	2.0V	2.0V	2.0V	Pulse	-800μA	6
"0" Output Voltage		0.2	0.4	V	0.8V	2.0V	2.0V	Pulse	16mA	7
"0" Input Current										
D_n	-0.2		1.2	mA	0.4V					
S_0 and S_1	-0.2		1.2	mA		0.4V	0.4V			
Clock	-0.2		1.6	mA				0.4V		
"1" Input Current										
D_n			40	μA	4.5V					
S_0 and S_1			40	μA		4.5V	4.5V			
Clock			40	μA				4.5V		

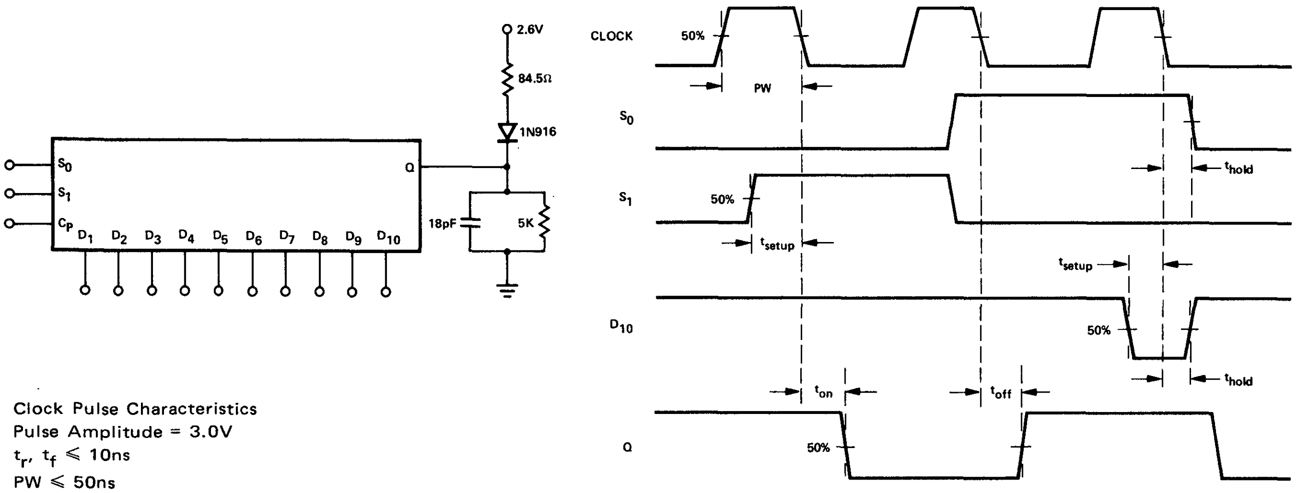
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	S_0	S_1	CLOCK	OUTPUT	
Data Transfer Rate	25	30		MHz						10
Turn-On Delay (Clock to Output)		27	40	ns						10
Turn-Off Delay (Clock to Output)		21	40	ns						10
Clock Pulse Width	20			ns						10
Set-Up Time (t_{setup})										10
D_n		6	10	ns						
S_0, S_1		16	25	ns						
Hold Time (t_{hold})										
D_n		2	5	ns						
S_0, S_1		16	25	ns						
Power Consumption		380	567	mW	4.5V	4.5V	4.5V	0V		8
Short Circuit Output Current	-20		-70	mA	2.0V	2.0V	2.0V	Pulse	0.0V	
Input Voltage Rating	5.5			V	10mA					

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. $V_{CC} = 5.25V$.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. See AC Test **Figure.**

AC TEST FIGURE AND WAVEFORMS



Clock Pulse Characteristics
Pulse Amplitude = 3.0V
t_r, $t_f \leqslant 10ns$
PW $\leqslant$ 50ns

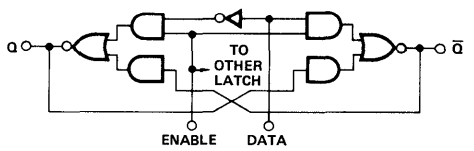
QUAD BISTABLE LATCH 8275

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8275 is a QUAD LATCH circuit designed to provide temporary storage of four bits of information. A common application is as a holding register between a counter and a display driver (such as the 8280 and 8T01.) Separate enable lines to latches 1-2 and 3-4 allow individual control of each pair of latches. Initially, data is transferred on the rising edge of the enable pulse. While the enable is high, output Q follows the data input. When the enable falls, the input data present at fall time is retained at the Q output. Both Q and $\overline{Q}$ are accessible.

LOGIC DIAGRAM AND TRUTH TABLE



Refer to Page 16 for Pin Configuration

(Each Latch)

ENABLE	DATA	Q	$\overline{Q}$
1	1	1	0
1	0	0	1
0	1	*	*
0	0	*	*

*No Change.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT	ENABLE INPUT	OUTPUTS	
"1" Output Voltage (Q, $\overline{Q}$)	2.6	3.5		V			-800μA	6, 11
"0" Output Voltage (Q, $\overline{Q}$)			0.4	V			16mA	7, 11
"0" Input Current (Data)	-0.1		-3.2	mA	0.4V	5.25V		
"0" Input Current (Enable)	-0.1		-6.4	mA	5.25V	0.4V		
"1" Input Current (Data)			80	μA	4.5V	0.0V		
"1" Input Current (Enable)			160	μA	0.0V	4.5V		

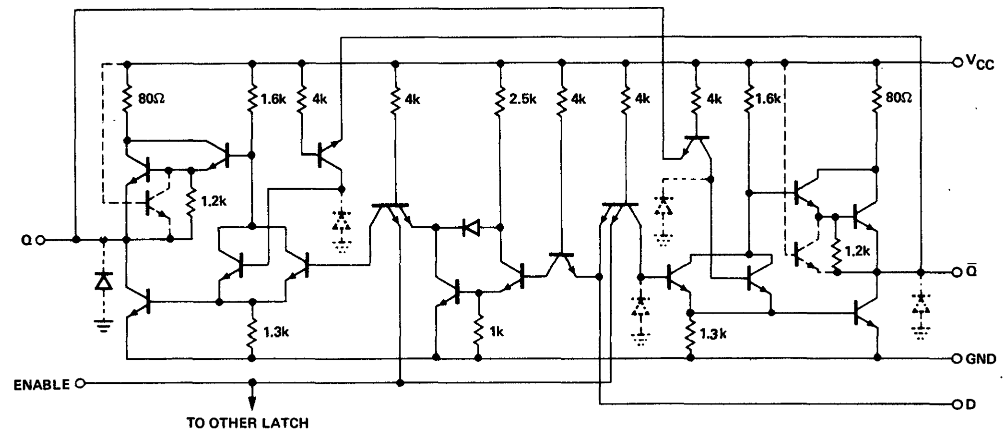
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT	ENABLE INPUT	OUTPUTS	
t_{setup} (1) at D input		12	20	ns				8, 12
t_{setup} (0) at D input		14	20	ns				8, 12
t_{hold} (1) at D input	0	15		ns				8, 13
t_{hold} (0) at D input	0	6		ns				8, 13
t_{pd} (1) D to Q		16	30	ns				8
t_{pd} (0) D to Q		14	25	ns				8
t_{pd} (1) D to $\overline{Q}$		24	40	ns				8
t_{pd} (0) D to $\overline{Q}$		7	15	ns				8
t_{pd} (1) E to Q		16	30	ns				8
t_{pd} (0) E to Q		12	20	ns				8
t_{pd} (1) E to $\overline{Q}$		16	30	ns				8
t_{pd} (0) E to $\overline{Q}$		12	20	ns				8
Power Consumption/Supply Current		205/39	265/50	mW/mA				14
Input Voltage Rating (Data)	5.5			V	10mA	0.0V		12
Input Voltage Rating (Enable)	5.5			V	0.0V	10mA		12
Output Short Circuit Current	-20		-70	mA	0.0V		0.0V	

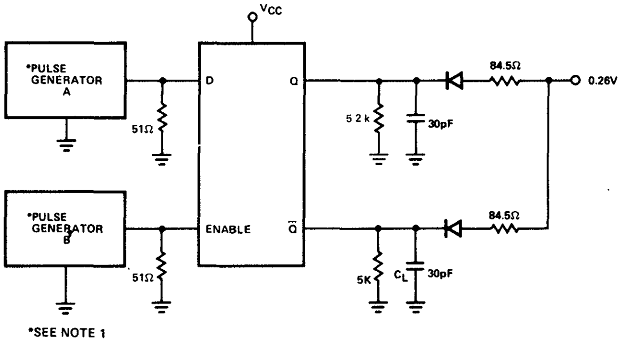
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Inputs for output voltage test is per TRUTH TABLE with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. t_{setup} is defined as the time prior to the fall of the clock.
13. t_{hold} is defined as the time after the fall of the clock.
14. V_{CC} = 5.25 volts.

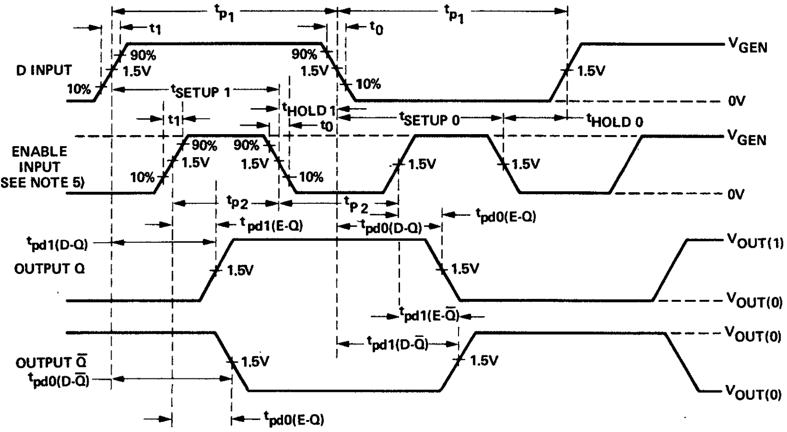
SCHEMATIC DIAGRAM



AC TEST FIGURES AND WAVEFORMS



AC TEST FIGURES AND WAVEFORMS (Cont'd)

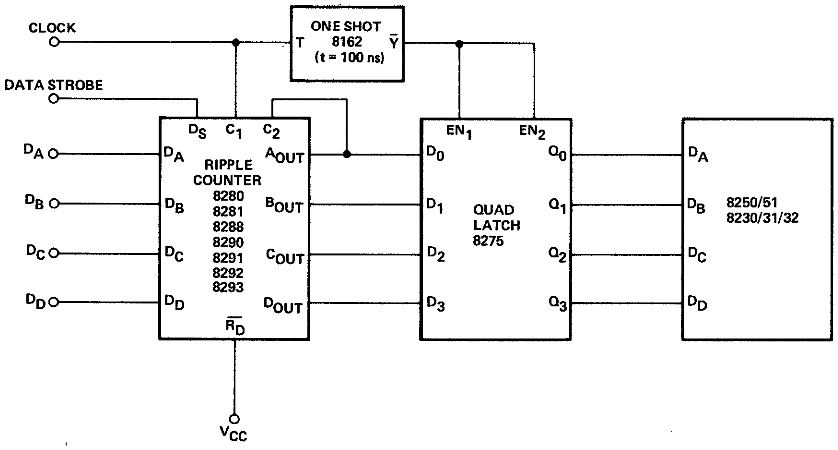


NOTES:

1. The pulse generators have the following characteristics: V_{gen} = 3V, $t_1 = t_0 \leqslant 10$ns, and $Z_{out} \approx 50\Omega$. For pulse generator A tp 1 = 1μs and PRR = 500kHz. For pulse generator B, tp2 = 500ns and Prr = 1MHz. Positions of D-input and enable input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.
5. When measuring $t_{pd}1$ (D-Q), $t_{pd}0$ (D-Q), $t_{pd}0$ (D-$\overline{Q}$), and $t_{pd}1$(D-$\overline{Q}$), enable input must be held at logical **1.**

TYPICAL APPLICATION

OUTPUT STROBING OF RIPPLE COUNTER TO ACHIEVE SYNCHRONOUS OUTPUT CHANGES



8-BIT SHIFT REGISTER 8276

PRODUCT AVAILABLE IN 0°C TO 75°C TEMP RANGE ONLY.

DIGITAL 8000 SERIES TTL/MSI

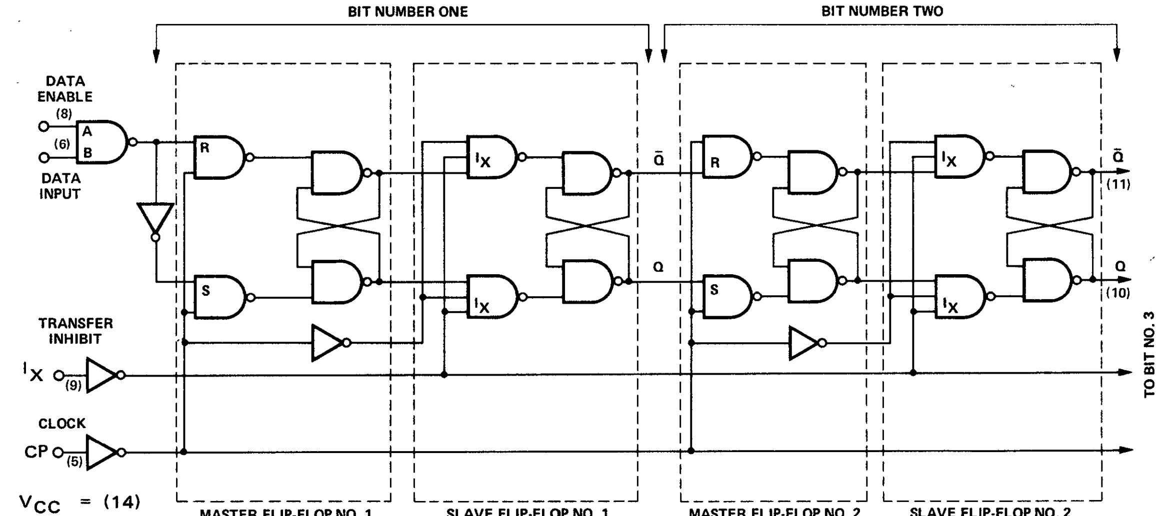
DESCRIPTION

The 8276 is a serial-in, serial-out 8-Bit Shift Register composed of eight R-S master slave flip-flops. This shift register has input gating and an internal clock driver. In addition, a data transfer inhibit input is provided.

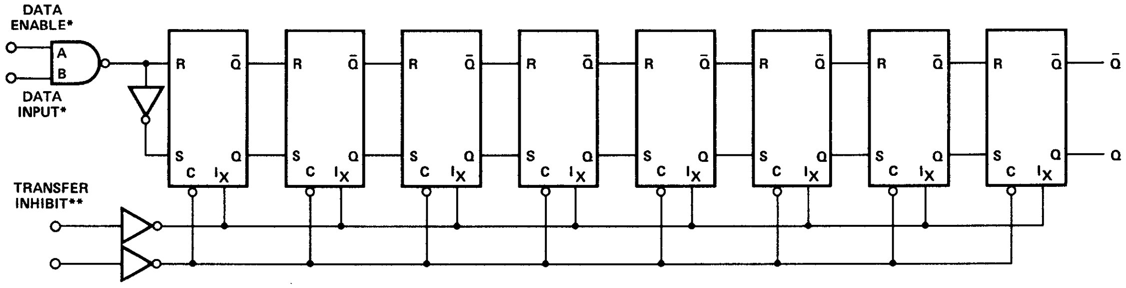
Data Input and Data Enable are gated through inputs A and B. An internal inverter provides the complimentary inputs to the first bit of the shift register. All inputs are fully buffered. Complementary Q and $\overline{Q}$ outputs are provided.

The internal clock driver/inverter causes the 8276 to shift data to the output on the positive edge of the input clock pulse, making the shift register compatible with the 8825 J-K Binary and the 8828 Dual D type Binary. The register is inhibited from shifting data when the Transfer Inhibit line is high. The inhibit function is achieved by preventing data transfer from master to slave sections of the register elements when the inhibit line is used.

LOGIC DIAGRAMS AND TRUTH TABLES



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers



t_n		t_{n+8}
A (Data Enable)	B (Data Input)	Q
0	0	0
0	1	0
1	0	0
1	1	1

*NOTE: These functions are interchangeable.
**NOTE: Transfer Inhibit prevents transfer of data from master to slave.

NOTES:
t_n = Bit time before clock pulse.
t_{n+8} = Bit time after 8 clock pulses.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUTS	CLOCK	TRANS. INHIBIT	OUTPUTS	
"1" Output Voltage Q	2.6			V	2.0V		0.8V	-800μA	6, 10
"1" Output Voltage $\overline{Q}$	2.6			V	0.8V		0.8V	-800μA	6, 10
"0" Output Voltage Q			0.4	V	0.8V		0.8V	16mA	7, 10
"0" Output Voltage $\overline{Q}$			0.4	V	2.0V		0.8V	16mA	7, 10
"0" Input Current									
Data Input	-0.1		-1.6	mA	0.4V				
Clock Input	-0.1		-1.6	mA		0.4V			
Inhibit Input	-0.1		-1.6	mA			0.4V		
"1" Input Current									
Data Inputs			40	μA	4.5V				
Clock Input			40	μA		4.5V			
Inhibit Input			40	μA			4.5V		
Input Voltage Rating	5.5			V	10mA	10mA	10mA		

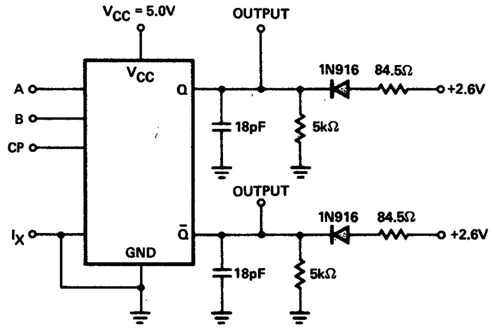
T_A = 25° C and V_{CC} = 5.0V

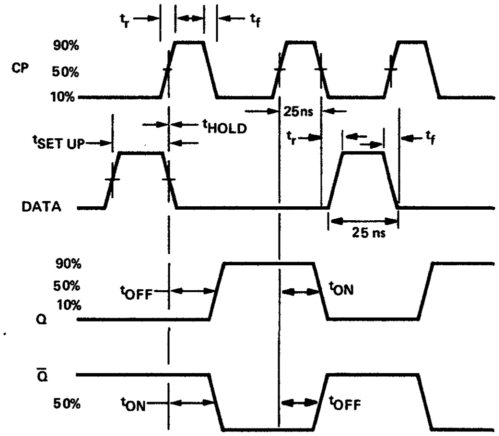
CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUTS	CLOCK	TRANS. INHIBIT	OUTPUTS	
Power/Current Consumption		205/39	340/65	mW/mA					11
Transfer Rate	15	20		MHz					
Turn-on Delay									
(Clock to Output)		22	33	ns					8
Turn-off Delay									
(Clock to Output)		22	33	ns					8
Clock Pulse Width	25			ns					
Set Up Time (Logical)									
"0" at A or B Input	25			ns					
Set Up Time (Logical)									
"1" at A or B Input	25			ns					
Output Short Circuit Current	-18		-55	mA				0V	

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Clock input is driven by a 1kHz square wave for at least 8 cycles prior to measurements.
11. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



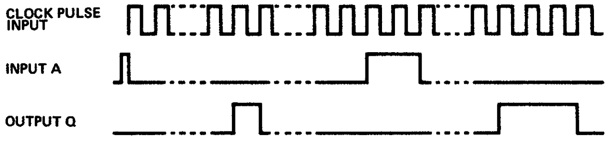


NOTES:
1. Unused input connected to 2.6V
2. Input pulse characteristics:
3. Setup time = 25ns
   Hold time = 0ns

CLOCK:
Amplitude = 3.0V
t_r = t_f = 5ns max
PRR = 15 MHz, Pulse width = 25ns at 50% points

INPUT:
Amplitude = 3.0V
t_r = t_f = 5ns max
PRR = 7.5 MHz
Pulse width = 25ns at 50% points

TYPICAL INPUT/OUTPUT WAVEFORMS



NOTE: Input B is connected to 2.6V. Transfer Inhibit Connected to 0V

DUAL 8-BIT SHIFT REGISTER 8277

PRODUCT AVAILABLE IN 0°C TO +75°C TEMP RANGE ONLY.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

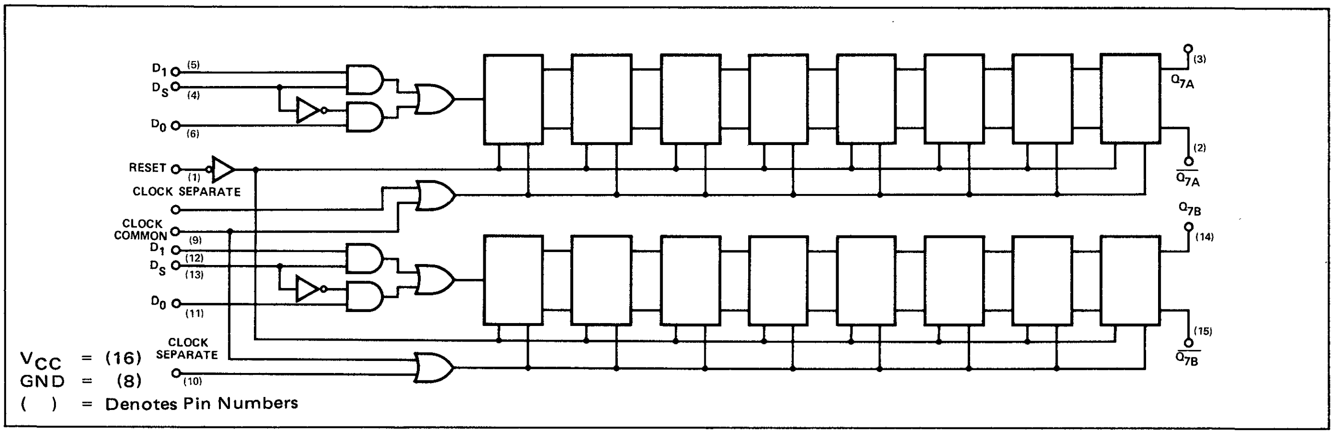
The 8277 is a dual 8-Bit Shift Register which provides the designer with sixteen (16) bits of serial storage operating at a typical shift rate of 20MHz. Features of the 8277 are:

1. TRUE and COMPLEMENT outputs are provided on each register's eighth bit.
2. Positive edge triggering on clock input.
3. SEPARATE CLOCK lines (pins 7 and 10) for each 8-bit register are provided as well as a COMMON CLOCK line (pin 9) for all sixteen storage bits.
4. Common RESET (pin 1).
5. AND-OR gating to the input of each 8-bit register is provided to accomplish the multiplex function.
6. Direct replacement for 9328.

TRUTH TABLE

D_S	D_0	D_1	Reset	Function
0	0	x	1	Shift in "0"
0	1	x	1	Shift in "1"
1	x	0	1	Shift in "0"
1	x	1	1	Shift in "1"
x	x	x	0	Reset "Q" to "0"

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

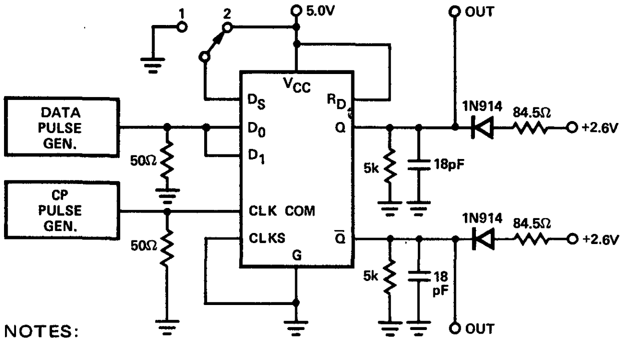
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA D_1, D_0	DATA SELECT	CLK COMMON	CLK SEP	RESET	OUTPUTS	
"1" Output Voltage (Q)	2.6	3.5		V	2.0V	2.0V	Pulse	0.8V	2.0V	-800μA	6
"1" Output Voltage (Q)	2.6	3.5		V	0.8V	2.0V	0.8V	Pulse		-800μA	6
"0" Output Voltage (Q)			0.4	V	0.8V	0.8V	Pulse	0.8V		16mA	7
"0" Output Voltage (Q)			0.4	V	2.0V	0.8V	Pulse	0.8V		16mA	7
"0" Input Current											
Data, Reset, Data Select			-1.6	mA	0.4V	0.4V			0.4V		
Clock Separate			-1.6					0.4V			
Clock Common			-3.2	mA			0.4V				
"1" Input Current											
Data, Reset, Clock Separate			40	μA	4.5V	4.5V		4.5V	4.5V		
Clock Common			80	μA			4.5V				
Power/Current Consumption			540/ 103	mW/ mA							11
Input Voltage Rating											
All Inputs	5.5			V	10mA	10mA	10mA	10mA	10mA		

$T_A = 25°C$ and $V_{CC} = 5.0V$

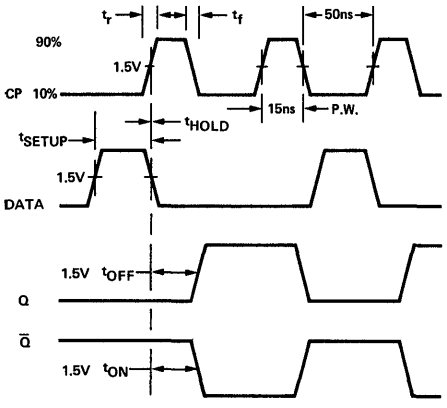
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA D_1, D_0	DATA SELECT	CLK COMMON	CLK SEP	RESET	OUTPUTS	
Turn-on Delay											
Clock To Output		25	40	ns							10
Reset To Output		25	40	ns							10
Turn-off Delay											
Clock To Output		25	40	ns							10
Reset To Output		25	40	ns							10
Clock Pulse Width	15			ns							10
Shift Rate	15	20		MHz							10
Data Set-up Time		20	30	ns							10
Data Hold Time		5	10	ns							10

NOTES:
1. All voltage measurments are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive Logic Definitions: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Manufacturer reserves the right to make design and process changes and improvements.
9. Clock input is driven by a 1kHz square wave for at least 8 cycles prior to measurement.
10. Refer to AC Test Figure.
11. $V_{CC} = 5.25V$

AC TEST FIGURE AND WAVEFORMS



NOTES:
1. Each register is tested separately.
2. All T delay measurements taken at 1.5V level.
3. Tie all unused inputs to 2.6V.
4. 18 pF on outputs includes probe and jug capacitance.

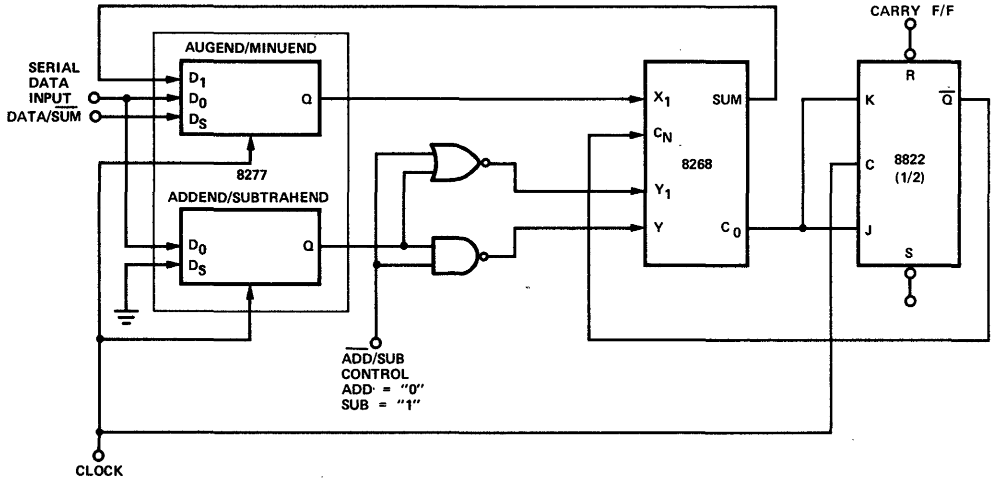


CLOCK PULSE:
P.A. = 3.0V
P.R.R. = 15 MHz
P.W. = 15 ns
$T_r = T_f = 5ns$

DATA PULSE:
P.A. = 3.0V
P.R.R. = 7.5 MHz
P.W. = 25 ns
$T_r = T_f = 5$ ns
$T_{SETUP} = 25$ ns
$T_{HOLD} = 0$ ns.

TYPICAL APPLICATION

8-BIT SERIAL ADD/SUBTRACTOR



BCD DECADE COUNTER/STORAGE ELEMENT
4-BIT BINARY COUNTER/STORAGE ELEMENT

8280
8281

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8280 Decade Counter and 8281 16-State Binary Counter are four-bit subsystems providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8280 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

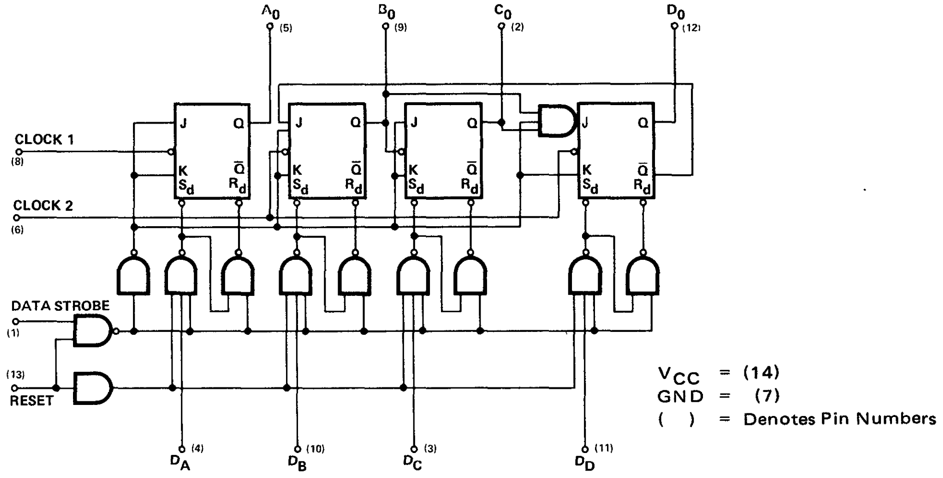
The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

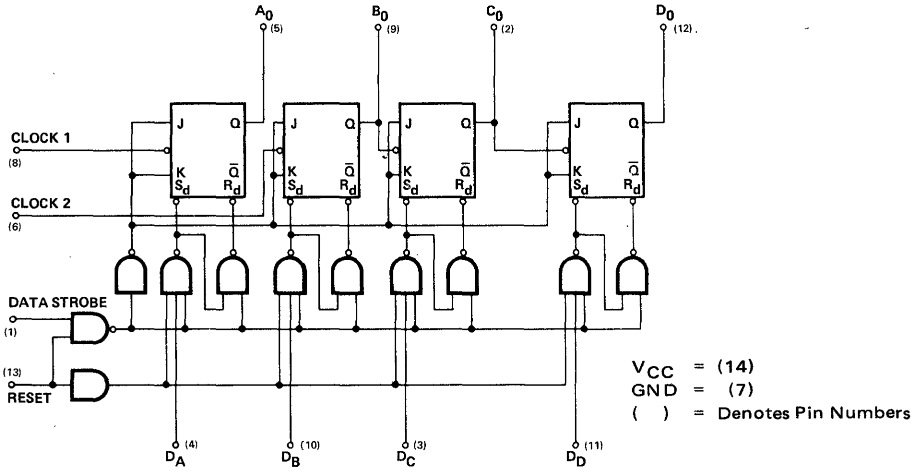
The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

LOGIC DIAGRAMS

8280



8281



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage (All Outputs)	2.6	3.5		V	0.8V	2.0V	2.0V		Output A	-800μA	7
"0" Output Voltage (All Outputs)			0.4	V	0.8V	0.8V	0.8V		Output A	16mA	8
"0" Input Current											
$\overline{\text{Strobe}}$	-0.1		-1.6	mA	0.4V						
Data Inputs	-0.1		-1.2	mA		0.4V					
$\overline{\text{Reset}}$	-0.1		-3.2	mA			0.4V				
Clock 1	-0.1		-3.2	mA				0.4V			
Clock 2 (8280)	-0.1		-3.2	mA					0.4V		
Clock 2 (8281)	-0.1		-1.6	mA					0.4V		
"1" Input Current											
$\overline{\text{Strobe}}$			40	μA	4.5V						
Data Inputs			40	μA		4.5V					
$\overline{\text{Reset}}$			80	μA			4.5V				
Clock 1			80	μA				4.5V			
Clock 2 (8280)			80	μA					4.5V		
Clock 2 (8281)			40	μA					4.5V		
Power/Current Consumption		184/35	236/45	mW/mA			0V	0V	0V		12
Input Voltage Rating all Inputs	5.5			V	10mA	10mA	10mA	10mA	10mA		10
Output Short Circuit Current	-10		-60	mA	0V					0V	

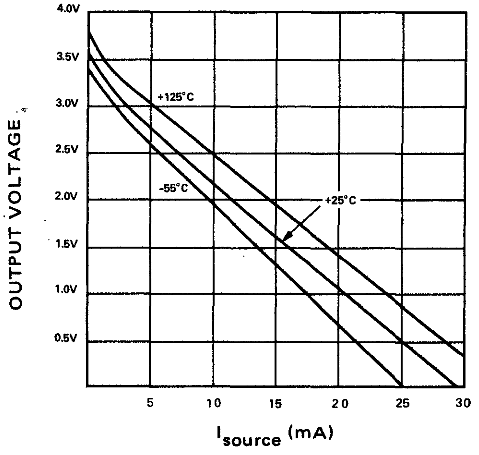
T_A = 25° C and V_{CC} = 5.0V

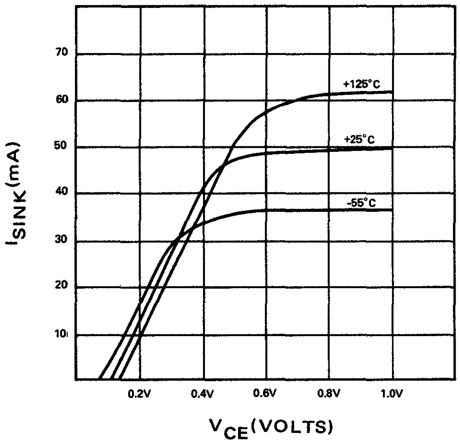
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Clock Mode T_{on} Delay											
Bit A, B, C, D		15	25	ns							11
Clock Mode T_{off} Delay											
Bit A, B, C, D		15	25	ns							11
Data/Strobe t_{on} Delay											
Bit A, B, C, D		25	35	ns							11
Data/Strobe t_{off} Delay											
Bit A, B, C, D		30	40	ns							11
Toggle Rate	20	25		MHz							11
$\overline{\text{Strobe}}$ Pulse Width		20	35	ns					A_{OUT}		11
$\overline{\text{Reset}}$ Pulse Width		20	35	ns					A_{OUT}		11
$\overline{\text{Strobe}}$ Release Time		30	40	ns					A_{OUT}		11
$\overline{\text{Reset}}$ Release Time		50	75	ns					A_{OUT}		11

NOTES:

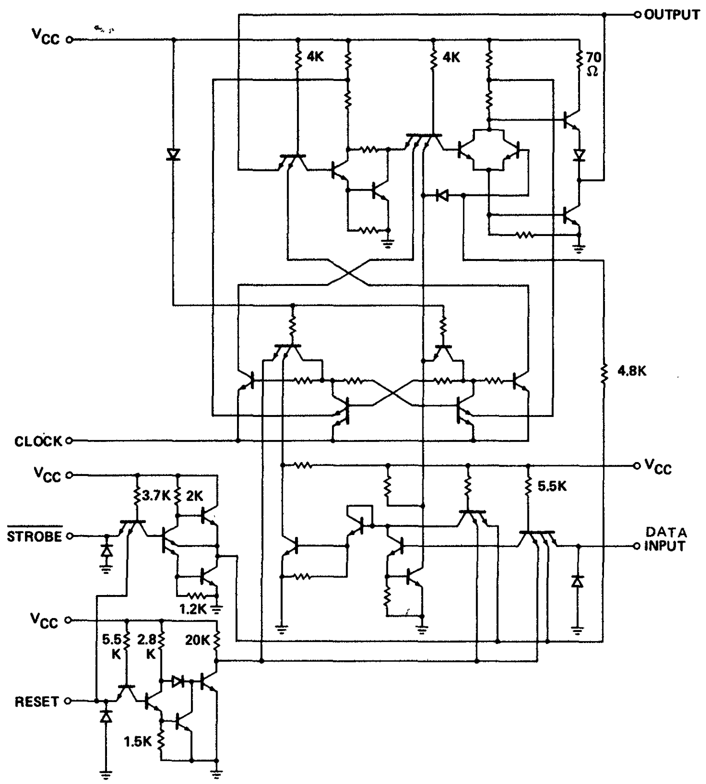
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Each input is tested separately.
11. Refer to AC Test Figures.
12. V_{CC} = 5.25V.

TYPICAL OUTPUT CHARACTERISTICS

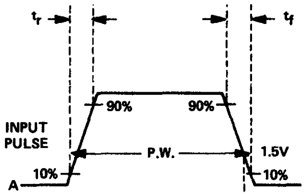




SCHEMATIC DIAGRAM

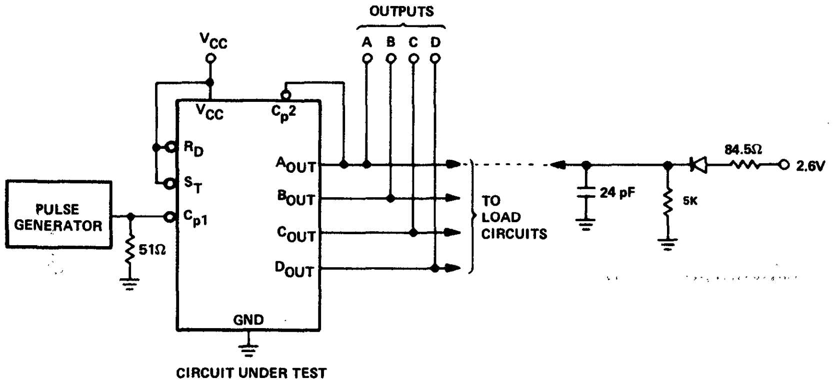


AC TEST FIGURES AND WAVEFORMS

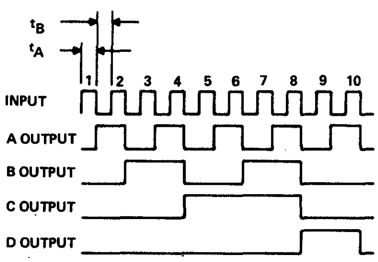


NOTE: Input pulse notations apply unless otherwise specified.

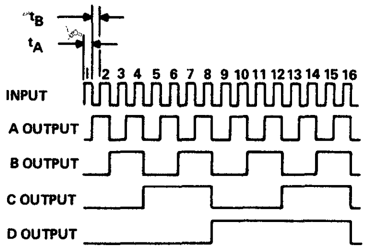
TOGGLE RATE



8280

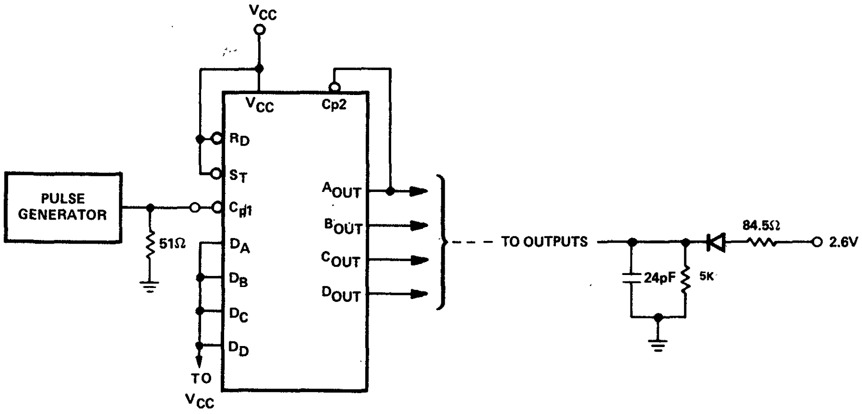


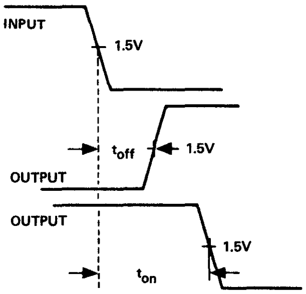
8281



INPUT PULSE:
Amplitude = 2.6V
t_A = 25ns, t_B = 25ns,
$t_r = t_f$ = 5ns max.

CLOCK MODE t_{on}/t_{off} DELAY



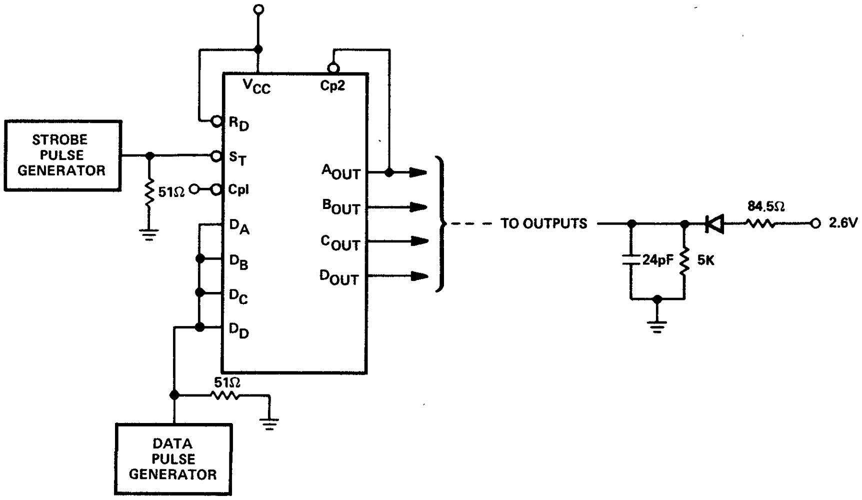


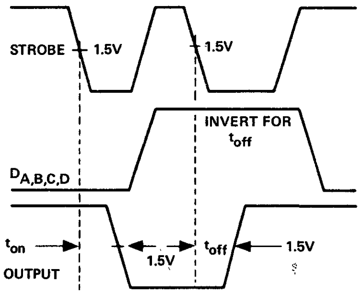
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:

INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns
$t_r = t_f$ = 5ns.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

DATA/STROBE t_{on}/t_{off}



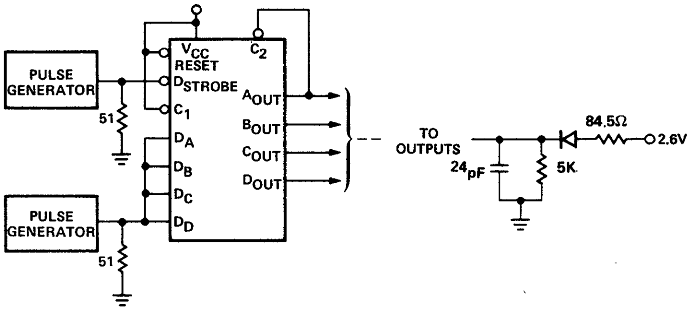


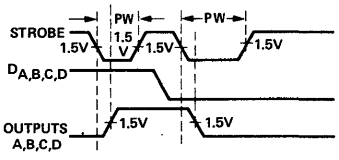
Strobe, P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1 MHz
t_r = t_f = 5ns
Data, P.A. = 2.6V
P.W. = 500ns
PRR = 500 KHz
t_r = t_f = 5ns.

NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25 mV_{rms}.
3. All diodes are 1N916.

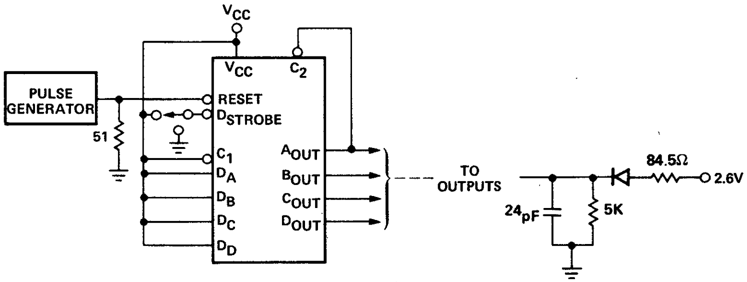
MINIMUM STROBE PULSE WIDTH

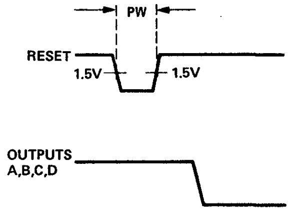




INPUT PULSE:
Amplitude = 2.6V
t_r = t_f = 5ns.

MINIMUM RESET PULSE WIDTH

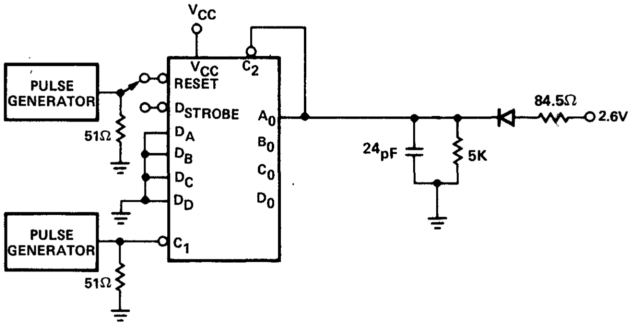


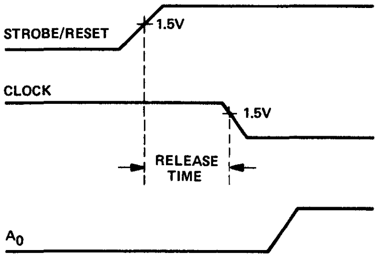


INPUT PULSE:
Amplitude = 2.6V
t_r = t_f = 5ns max.
Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

STROBE/RESET RELEASE TIME





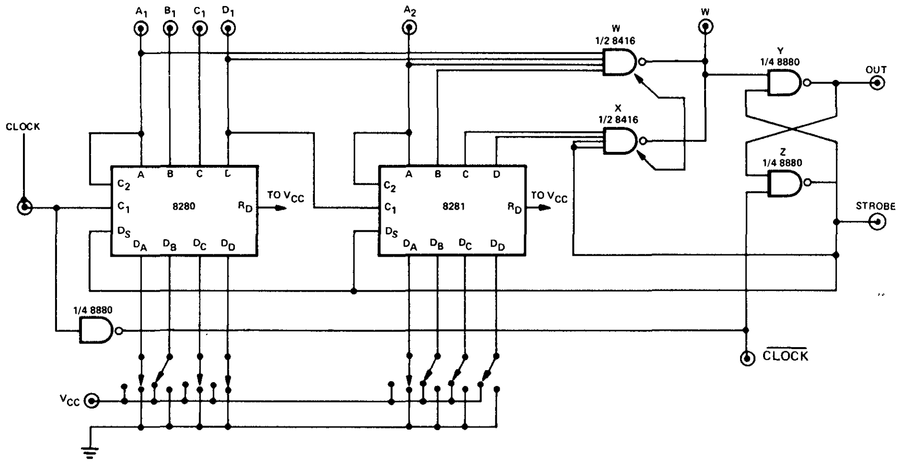
NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, $V_{ac} = 25mV_{rms}$.
3. All diodes are 1N916.

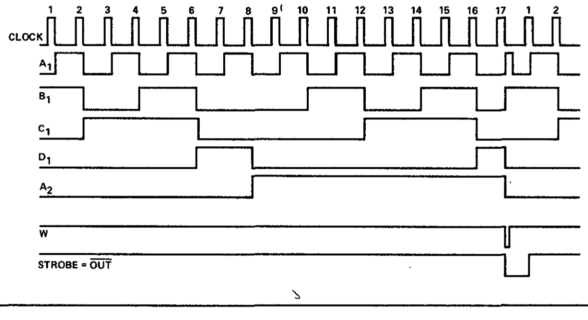
Clock, Strobe/Reset:
Ampl = 2.6V
tr = tf = 5 ns max.
PRR = 1 MHz 50% Duty Cycle.

TYPICAL APPLICATIONS

VARIABLE MODULUS COUNTER



TIMING DIAGRAM



BINARY HEXADECIMAL AND BCD DECADE, SYNCHRONOUS UP/DOWN COUNTERS

8284
8285

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The Up/Down Counter is a monolithic MSI circuit containing gates and binaries interconnected to provide a bidirectional divide-by-ten (decade) or divide-by-sixteen (hexadecimal) result as a function of the clock input.

The output code of the decade up/down counter is the commonly used BCD (8421) code, and the output sequence generated is the binary equivalent of the decimal numbers 0 through 9.

The hexadecimal up/down counter provides the output sequence 0 through 15 which is presented in a weighted binary code (8421).

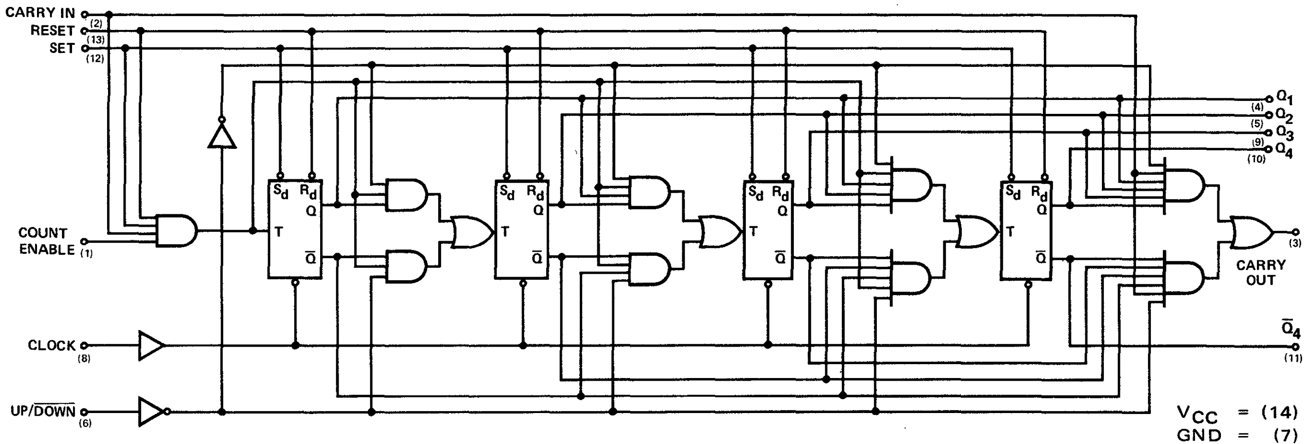
Set and Reset on the binary elements provide asynchronous entry with respect to the clock line, causing a count of "0" or "15" (8284) or of "0" or "9" (8285), and also inhibit propagation of count enable data.

Entry and propagation of data is performed in a synchronous manner with the clock line, which is active on its negative going excursion. The input from a previous stage or other source is channeled through "Carry In" and its propagation can be inhibited by the "Count Enable" line. "Carry In" and "Count Enable" input duality gives added flexibility in multiple package cascading applications.

Direction of the counter is steered from a single line (Up/$\overline{\text{Down}}$), where a "0" level will cause a "down" count and a "1" level will accomplish an "up" count.

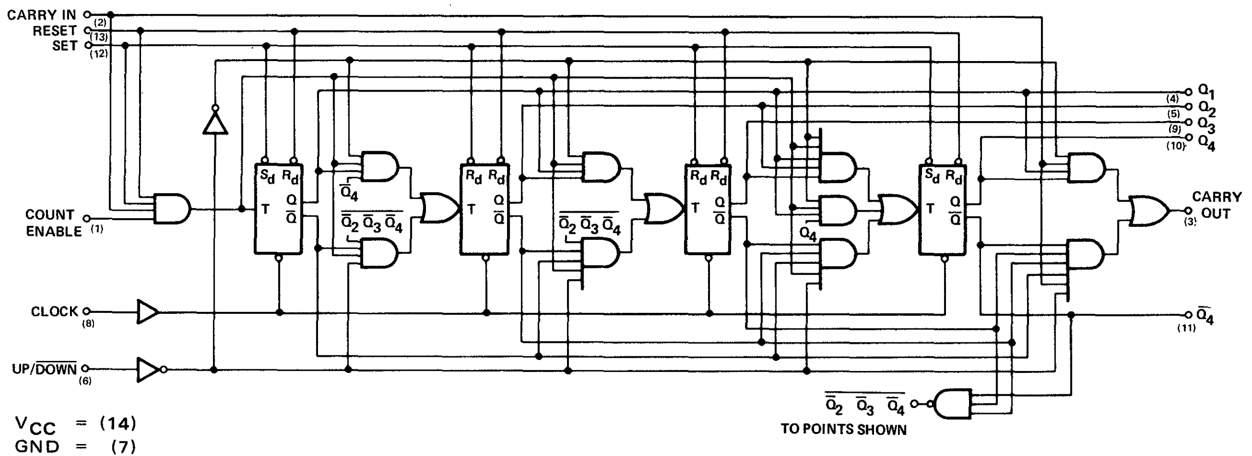
All Q outputs of the four binaries are brought to the outside world, together with the $\overline{Q}$ output of the most significant binary (Q4) and the Carry Out.

LOGIC DIAGRAMS



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

(8284)



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

(8285)

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	SET	RESET	UP/DOWN	COUNT ENABLE	CLOCK	CARRY IN	OUTPUTS	
"1" Output Voltage												
Q_1, Q_4, Carry Out	2.6			V	0.8V	2.0V	2.0V			2.0V	-800µA	
Q_2, Q_3, (8284)												
Q_2, Q_3 (8285)	2.6			V	Pulse		0.8V				-800µA	
Q4	2.6			V	2.0V	0.8V					-800µA	
"0" Output Voltage												
Q_1,Q_2,Q_3,Q_4 and Carry Out			0.4	V	2.0V	0.8V				0.8V	9.6mA	
$\overline{Q}_4$			0.4	V	0.8V	2.0V					9.6mA	
"1" Input Current												
Carry In			120	µA	Pulse		5.0V			4.5V		
Set			200	µA	4.5V	Pulse						
Reset			40	µA	Pulse	4.5V						
Count Enable			40	µA				4.5V				
Clock and Up/Down			40	µA			4.5V		4.5V			
"0" Input Current												
Carry In			3.2	mA	Pulse		0V			0.4V		
Set			6.4	mA	0.4V							
Reset			6.4	mA		0.4V						
Count Enable			1.6	mA				0.4V				
Clock			1.6	mA					0.4V			
Up/Down			1.6	mA			0.4V					
Input Latch Voltage												
Carry In	5.5			V		0V	5.0V	0V		10mA		
Reset	5.5			V		10mA		0V		0V		
Set	5.5			V	10mA			0V		0V		
Count Enable	5.5			V	0V			10mA		0V		
Up/Down	5.5			V			10mA					
Output Short Circuit Current	-20		-70	mA							0V	

T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	SET	RESET	UP/DOWN	COUNT ENABLE	CLOCK	CARRY IN	OUTPUTS	
Power Consumption		315	420	mW								12
Propagation Delay												
t_{on} Clock to Q_4 & $\overline{Q}_4$		32	45	ns								7
t_{on} Clock to Q_1, Q_2, Q_3		28	40	ns								7
t_{off} Clock to Q_n, $\overline{Q}_n$		25	35	ns								7
t_{on} Reset to Q_n		24	35	ns								7
t_{off} Set to Q_n		15	25	ns								7
t_{on} Reset to $\overline{Q}_n$		32	45	ns								7
t_{on} Carry In to Carry Out		15	25	ns								7
t_{off} Carry In to Carry Out		20	30	ns								7
Clock Min. "1" Interval	20	15		ns								7
Count Rate	20	30		MHz								
Carry In, Count Enable, & Up/Down Set-Up Time		15	25	ns								
Carry In, Count Enable & Up/Down Hold Time		0	2	ns								
Set/Reset Pulse Width		20	25	ns								

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Output source current is supplied through a resistor to ground.
6. Output sink current is supplied through a resistor to V_{CC}.
7. Refer to AC Test Figure.
8. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Connect Q_4 to count enable, set the counter (1001), and count down. The counter will halt at BCD-7 (0111).
11. Pulse is normally at +4.0 volts, falling to 0 volts for at least 100 nsec.
12. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

MODE OF OPERATION

8284 Binary Synchronous Up/Down Counter
8285 BCD Synchronous Up/Down Counter

	SET	RESET	CARRY IN	COUNT ENABLE	UP/$\overline{\text{DOWN}}$	FUNCTION
A. Asynchronous						
	1	0	X	X	X	"0" (0 0 0 0)
8284 Only	0	1	X	X	X	"15" (1 1 1 1)
8285 Only	0	1	X	X	X	"9" (1 0 0 1)
B. Synchronous						
	1	1	0	X	X	Hold *
	1	1	X	0	X	Hold *
	1	1	1	1	0	"Down" Count *
	1	1	1	1	1	"Up" Count *

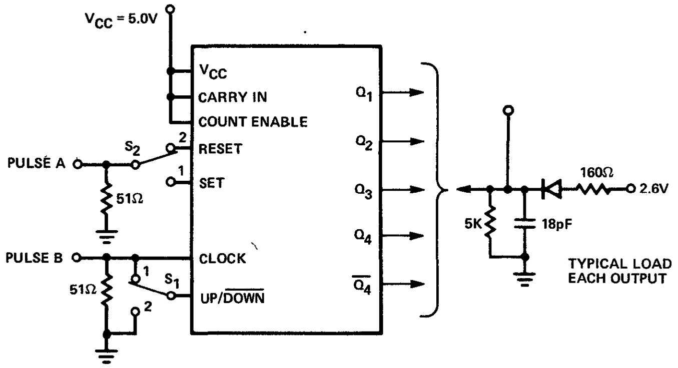
*Function is synchronous with NEGATIVE going transition of the Clock pin.
X = don't care.

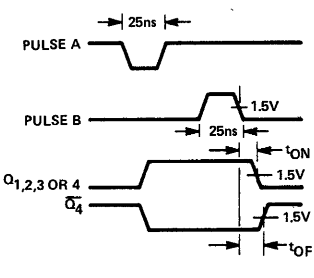
CARRY OUT

Carry Out_{8284} = Carry In $(Q_1 Q_2 Q_3 Q_4\ \text{UP} + \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{Q}_4\ \overline{\text{DOWN}}$

Carry Out_{8285} = Carry In $(Q_1 Q_4\ \text{UP} + \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{Q}_4\ \overline{\text{DOWN}}$

CLOCK MODE (t_{on} AND t_{off})

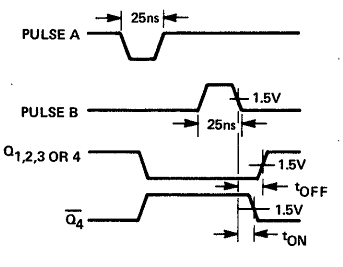




Reset Tied To V_{CC}
S_1' Position 1
S_2' Position 1

PULSE A

Pulse Amplitude = 2.6V
Pulse Width$_{(0)}$ = 25ns at 1.5V
Frequency = 5 MHz
$t_r = t_f$ = 5ns at 10% to 90% Points



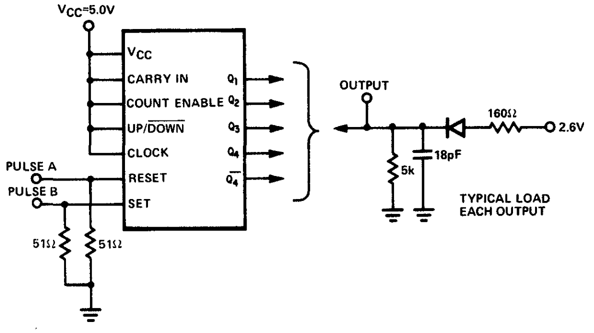
Set Tied To V_{CC}
S_1' Position 2
S_2' Position 2

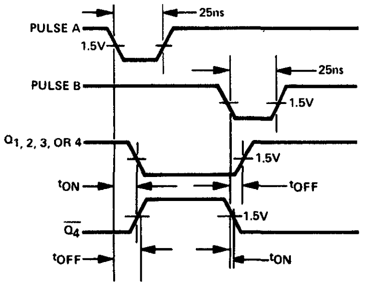
PULSE B

Pulse Amplitude = 2.6V
Pulse Width = 25ns at 1.5V
Frequency = 5 MHz
$t_r = t_f$ = 5ns at 10% to 90% Points

AC TEST FIGURES AND WAVEFORMS (Cont'd)

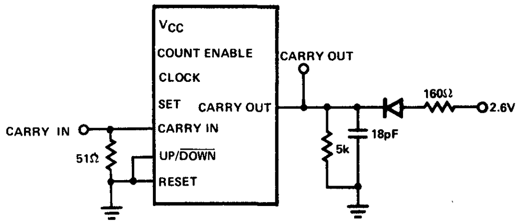
SET/RESET MODE (t_{on} and t_{off})

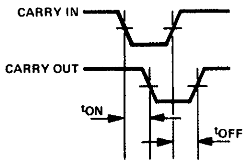




Pulse A and B
Pulse amplitude = 2.6V
Pulse width (0) =25ns
Frequency = 5MHz
$t_r = t_f$ =5ns at 10% to 90% points

CARRY IN/CARRY OUT (t_{on} and t_{off})

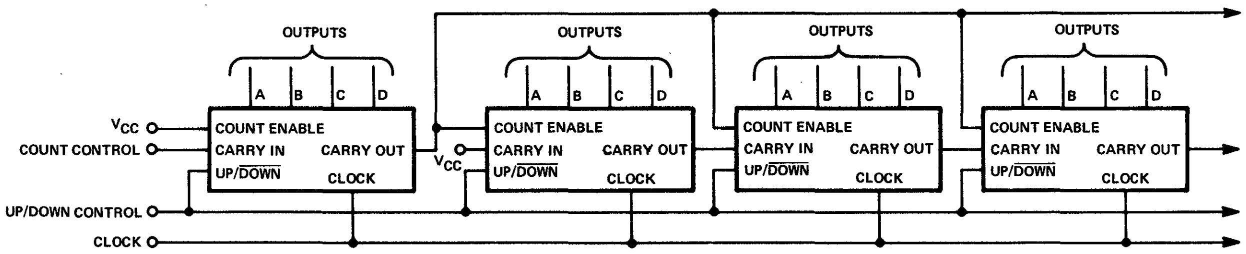




Carry in pulse
Pulse amplitude = 2.6V
Pulse width (0) = 50ns
Frequency =10MHz
$t_r = t_f$ =5ns at 10% to 90% points

TYPICAL APPLICATIONS

SYNCHRONOUS EXPANSION UP/DOWN COUNTERS



DIVIDE-BY-TWELVE COUNTER/STORAGE ELEMENT

8288

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8288 Divide by Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

The 8288 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, the 8288 is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

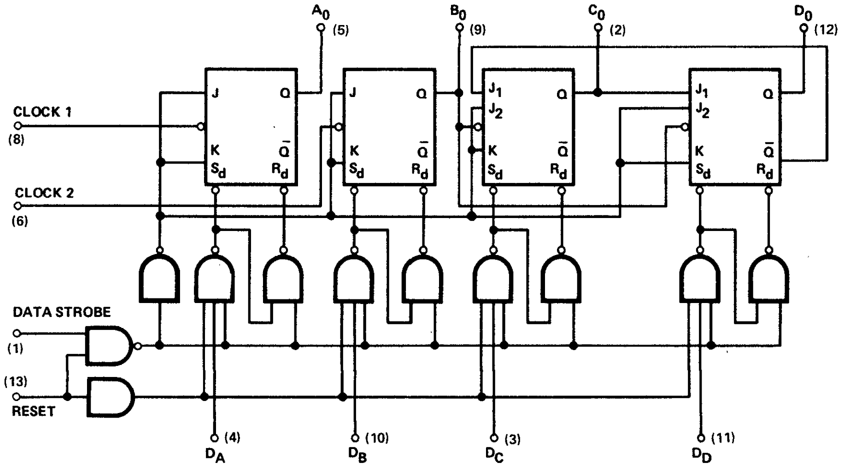
The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset functions are asynchronous with respect to the clock. The 8288 is compatible with all Signetics 8000 series elements.

TRUTH TABLE*

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

*Connected for Divide-by-Twelve operation (output A connected to CP2)

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7) A,F PACKAGES
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V		Output A	800μA	6, 7
"0" Output Voltage			0.4V	V	0.8V	0.8V	0.8V		Output A	16mA	6, 8
"0" Input Current											
Data Strobe	–0.1		–1.6	mA	0.4V		5.25V				
Data Inputs	–0.1		–1.2	mA		0.4V					
Reset	–0.1		–3.2	mA	5.25V		0.4V				
Clock 1	–0.1		–3.2	mA				0.4V			
Clock 2	–0.1		–1.6	mA					0.4V		
"1" Input Current											
Data Strobe			40	μA	4.5V		0V				
Data Input			40	μA		4.5V					
Reset			80	μA			4.5V				
Clock 1			80	μA				4.5V			
Clock 2			80	μA					4.5V		
Power/Current Consumption		184/35	236/45	mW/mA			0V	0V	0V		11
Input Voltage Rating											
Data Strobe	5.5			V	10mA						
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				
Output Short Circuit Current	–10		–60	mA	0V					0V	

$T_A = 25°C$ and $V_{CC} = 5.0V$

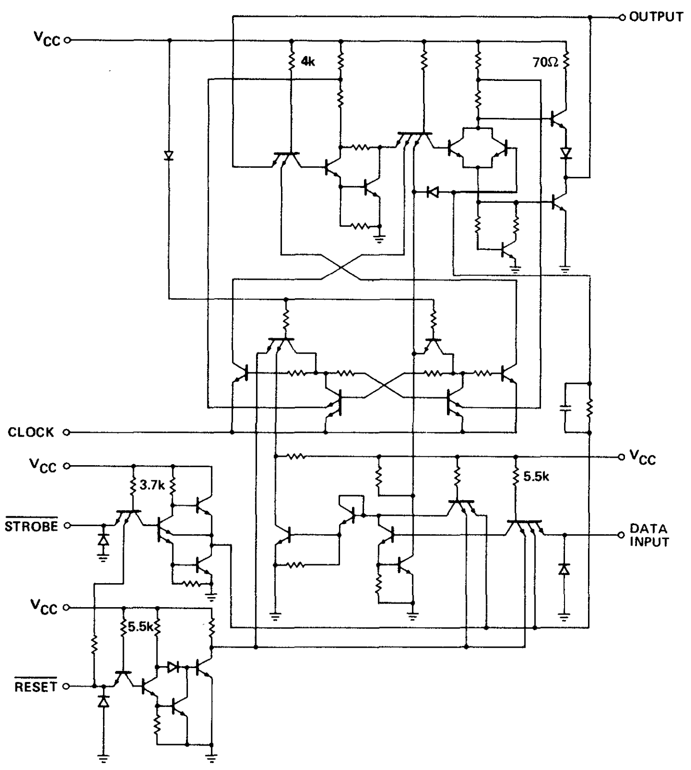
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Clock Mode t_{on} Delay											
Bit A, B, C, D		15	25	ns							9
Clock Mode t_{off} Delay											
Bit A, B, C, D		15	25	ns							9
Data/Strobe t_{on} Delay											
Bit A, B, C, D		20	35	ns							9
Data/Strobe t_{off} Delay											
Bit A, B, C, D		25	40	ns							9
Toggle Rate	20	25		MHz							9
Strobe Hold Time		25	35	ns		0.8V	2.0V	2.0V	Output A		
Reset Hold Time		20	35	ns	2.0V	0.8V		2.0V	Output A		
Strobe Release Time		30	40								
Reset Release Ti me		50	75	ns							

NOTES:

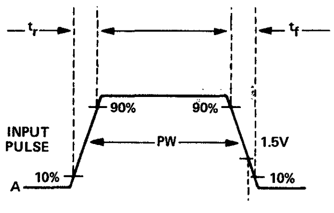
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM

8288 BASIC BINARY



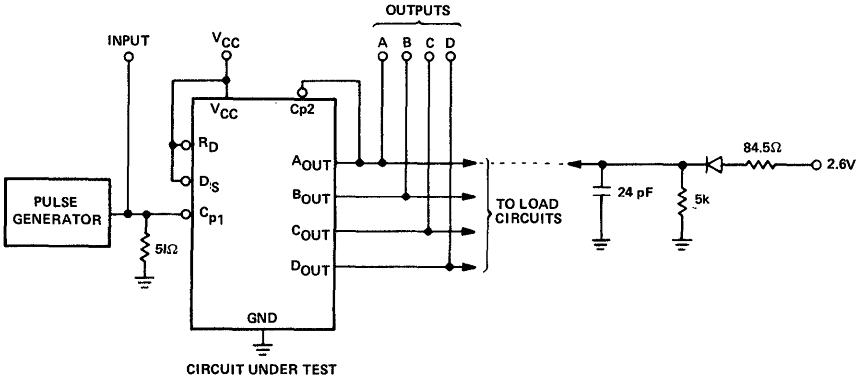
AC TEST FIGURES AND WAVEFORMS

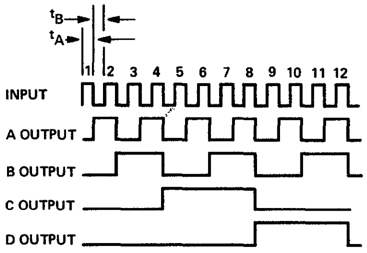


NOTE: Input pulse notations apply unless otherwise specified.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

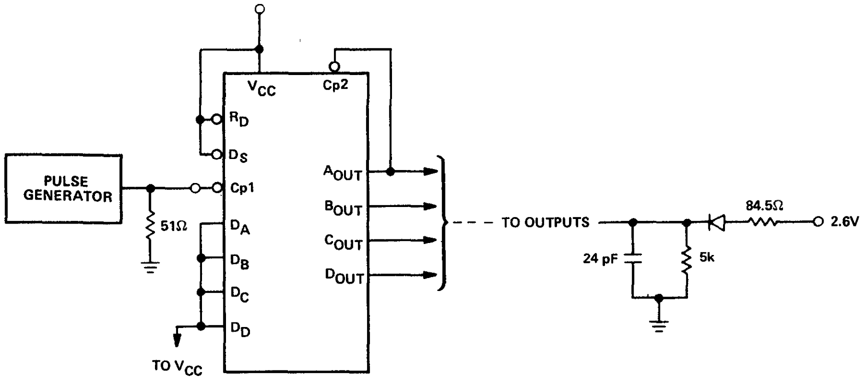
TOGGLE RATE

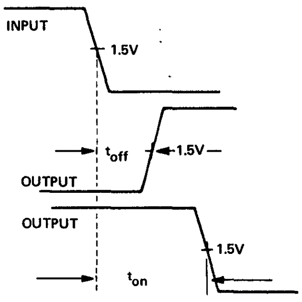




INPUT PULSE:
Amplitude = 3.4V
t_A = 100ns
t_r = 20ns
t_B = 300ns

CLOCK MODE t_{on}/t_{off} DELAY



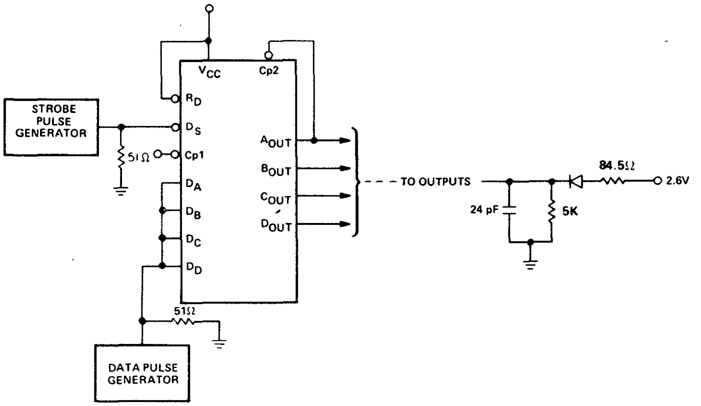


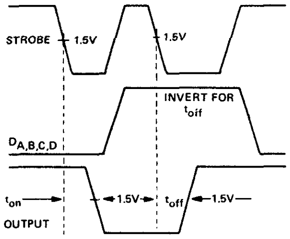
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:

INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns
t_r = t_f = 5ns

AC TEST FIGURES AND WAVEFORMS (Cont'd)

DATA/STROBE t_{on} t_{off}

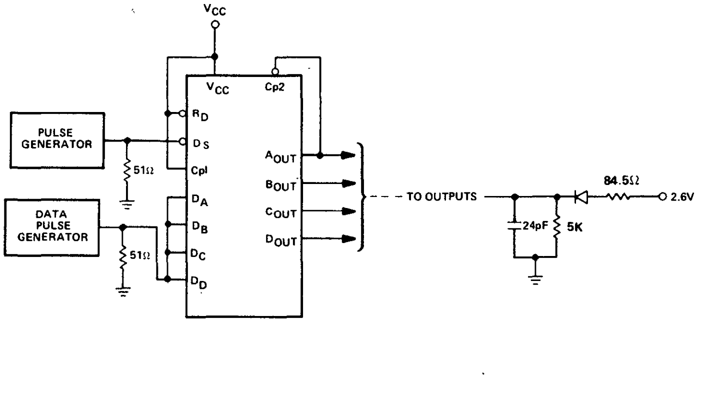


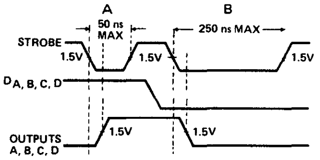


NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25 mF_{rms}.
3. All diodes are 1N914.

STROBE HOLD TIME





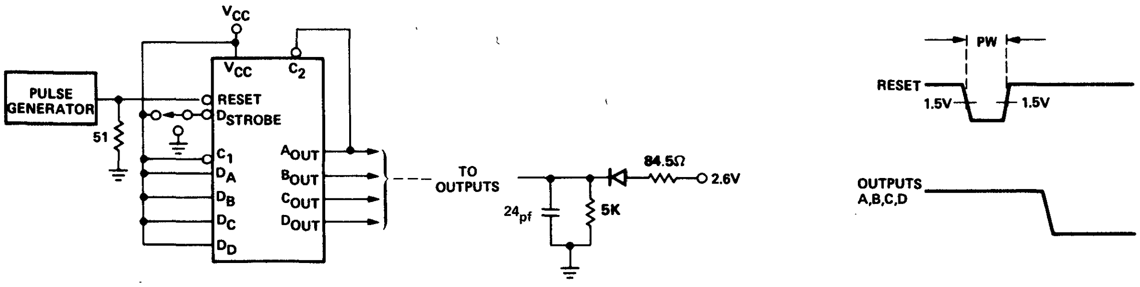
A With all outputs initially "0", output shall have a "0" to "1" transition.

B With all outputs initially "1", outputs shall have a "1" to "0" transition.

Amplitude = 2.6V (from Pulse Generator)
$t_r = t_f$ = 50 ns

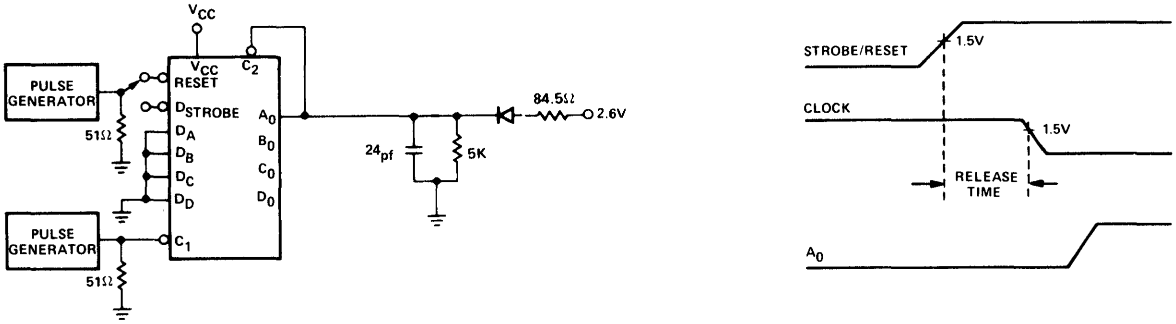
AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM RESET PULSE WIDTH



INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f = 5\text{ns}$ max.
Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

STROBE/RESET RELEASE TIME



Clock, Strobe/Reset Amplitude = 2.6V
$t_r = t_f = 5\text{ns}$ max. PRR = 1MHz 50% Duty Cycle.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, $V_{ac} = 25mV_{rms}$.
3. All diodes are 1N916.

PRESETTABLE HIGH SPEED DECADE/BINARY COUNTER

8290
8291

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8290 Decade Counter and 8291 Binary Counter are high speed devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8290 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8291 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

The counting operation is performed on the falling (negative going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

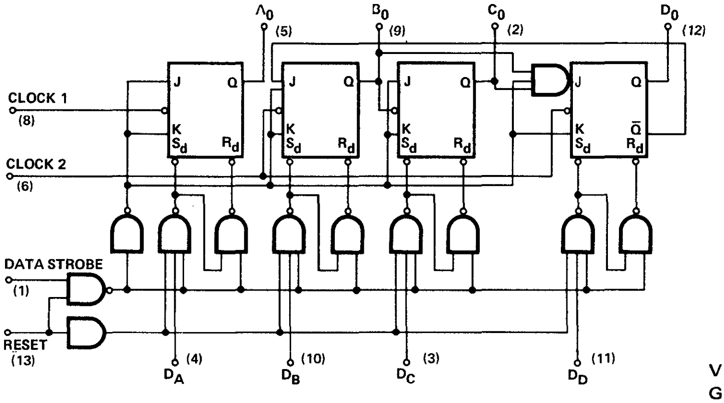
The various counter arrangements, as well as additional applications suggestions may be found in the Signetics Handbook "DESIGNING WITH MSI—Counters and Shift Registers Vol. 1.

LOGIC DIAGRAMS AND TRUTH TABLES

8290

Bi-Quinary (5-2)				
Input	B_0	C_0	D_0	A_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	1

V_{CC} = (14)
GND = (7)
A,F PACKAGES
( ) = Denotes Pin Numbers

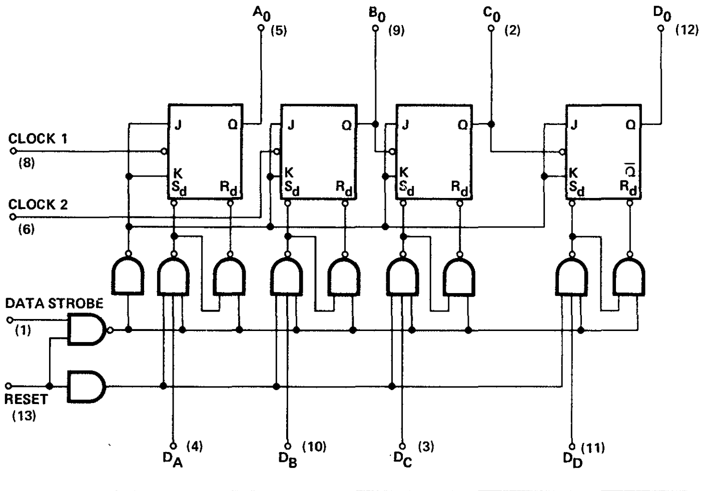


Decade (BCD)				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

V_{CC} = (4)
GND = (11)
W PACKAGE
( ) = Denotes Pin Numbers

8291

Binary				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1



V_{CC} = (4)
GND = (11)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V			-200µA	6, 8
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V			9.6mA	6, 9
"0" Input Current											
Data Strobe	-0.1		-1.6	mA	0.4		5.25V				
Data Inputs	-0.1		-1.2	mA		0.4					
Reset	-0.1		-2.8	mA	5.25V		0.4				
Clock 1	-0.1		-4.8	mA	5.25V			0.4			
Clock 2 (8290)	-0.1		-4.8	mA	5.25V				0.4		
Clock 2 (8291)	-0.1		-2.4	mA	5.25V				0.4		
"1" Input Current											
Data Strobe			40	µA	4.5V		0.0V				
Data Inputs			40	µA		4.5V					
Reset			80	µA	0.0V		4.5V				
Clock 1			80	µA	0.0V			4.5V			
Clock 2 (8290)			120	µA	0.0V				4.5V		
Clock 2 (8291)			80	µA	0.0V				4.5V		
Output Short Circuit Current A	-20		-70	mA						0.0V	13
B, C, D	-10		-60	mA	0.0V					0.0V	13
Input Voltage Rating											
Data Strobe	5.5			V	10mA						
Clock 1 & 2	5.5			V				10mA	10mA		
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				

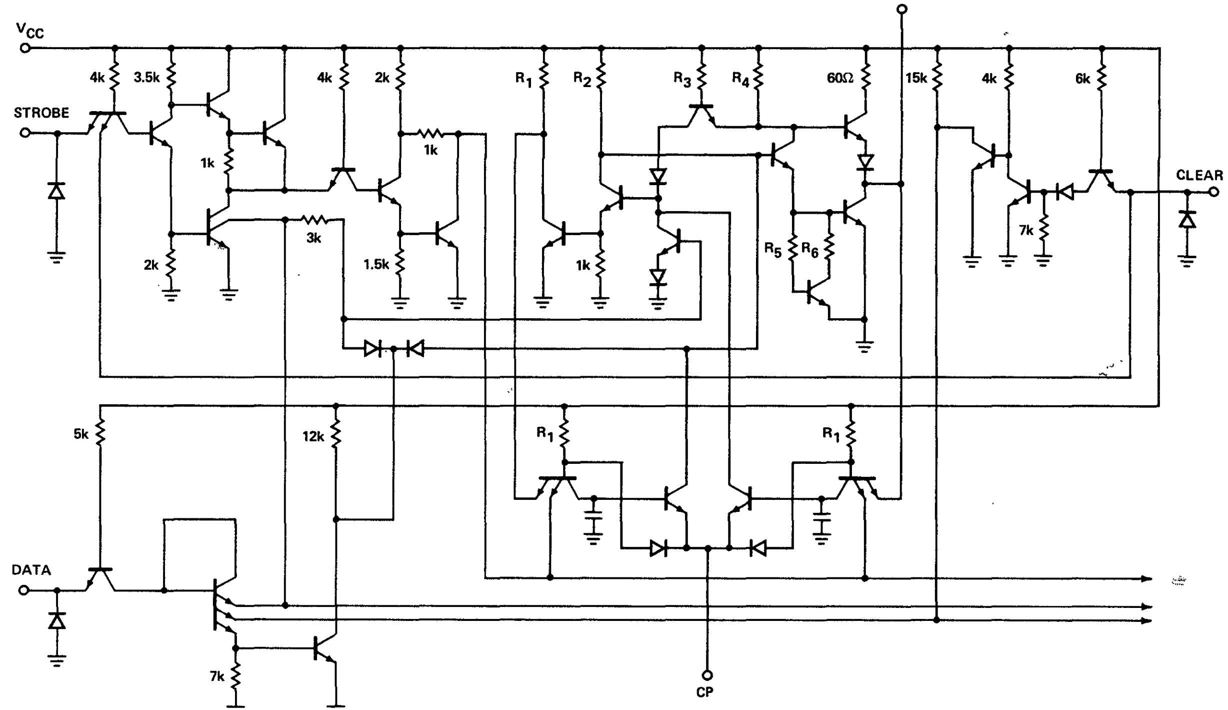
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Power Consumption/		190/	255/	mW/			0.0V	0.0V	0.0V		13
Supply Current		36.5	48.5	mA							
Strobe Pulse Width		15		ns					A_{OUT}		9
Reset Pulse Width		25		ns					A_{OUT}		9
Strobe/Reset Release Time		20		ns					A_{OUT}		9
Clock Mode t_{on} Delay											
Bit A		12	25	ns							9
Bits B, C, D		15	30	ns							9
Clock Mode t_{off} Delay											
Bit A		12	23	ns							9
Bits B, C, D		15	25	ns							9
Strobed Data t_{on} Delay (All Bits)		31	42	ns							9
Strobed Data t_{off} Delay (All Bits)		33	42	ns							9
Toggle Rate	40	60		MHz							9
Clock Mode Switching Test			75	ns							9, 11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. This test guarantees the device will reliably trigger on a pulse with 75ns fall-time.
12. Not more than one output should be shorted at a time.
13. V_{CC} = 5.25V.

SCHEMATIC DIAGRAM

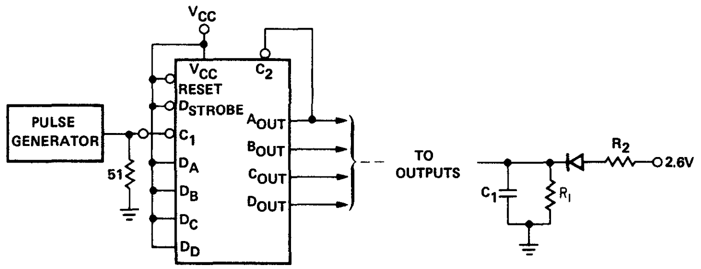


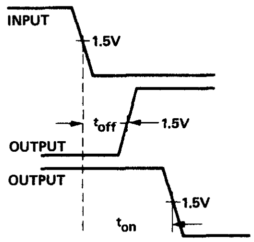
RESISTOR VALUES

	BIT A	BIT B,C,D
R_1	2.5k	5k
R_2	3.2k	5.5k
R_3	2k	5k
R_4	800Ω	3.5k
R_5	45Ω	355Ω
R_6	200Ω	1.15k

AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY



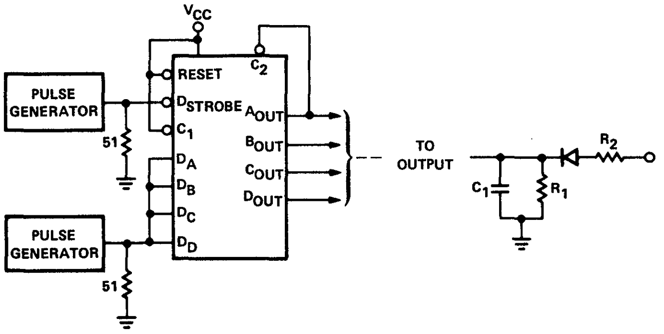


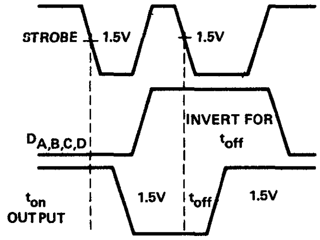
Note:
t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.

INPUT PULSE:
Amplitude = 2.6V
PW = 30ns, 50% to 50%
$t_r = t_f = 5ns$
PRR = 1MHz

AC TEST FIGURES AND WAVEFORMS (Cont'd)

STROBED DATA t_{on}/t_{off} DELAY

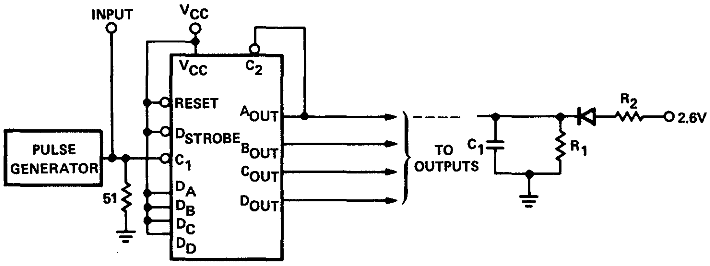




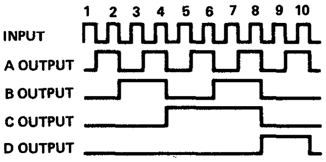
STROBE, PA = 2.6V
PW = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f = 5ns$

DATA, PA = 2.6V
PW = 500ns, 50% to 50%
PRR = 500kHz
$t_r = t_f = 5ns$

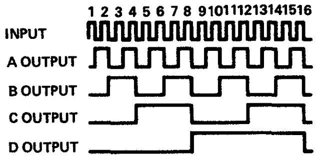
CLOCK MODE SWITCHING TEST



8290



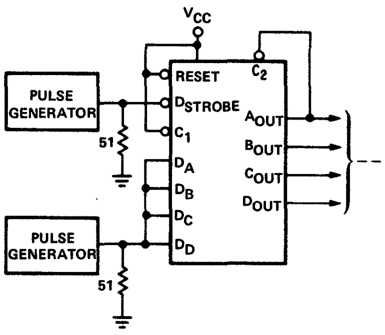
8291

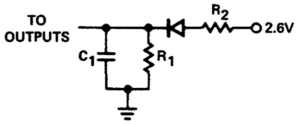


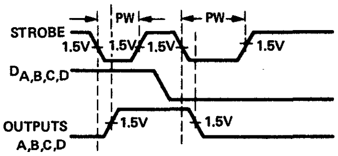
INPUT PULSE:
Amplitude = 3.4V
PW = 100ns, 50% to 50%
PRR = 2.5MHz
$t_r = 20ns$, $t_f = 75ns$

AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM STROBE PULSE WIDTH





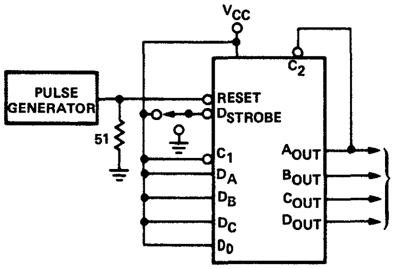


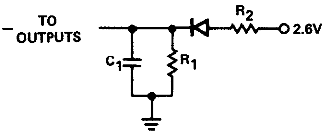
INPUT PULSE:

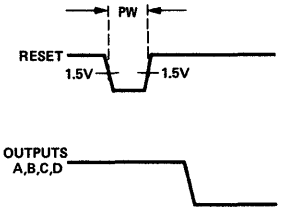
Amplitude = 2.6V

$t_r = t_f = 5ns$

MINIMUM RESET PULSE WIDTH



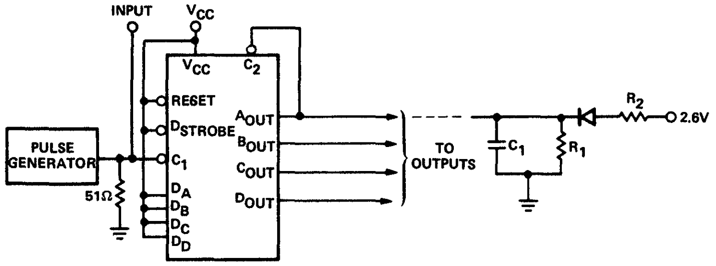


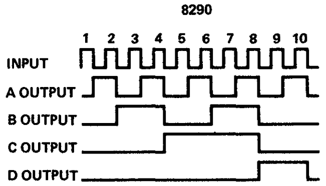


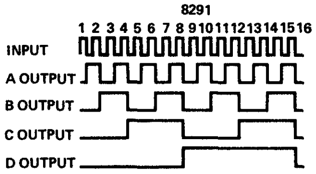
INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f = 5ns$.
Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

TOGGLE RATE

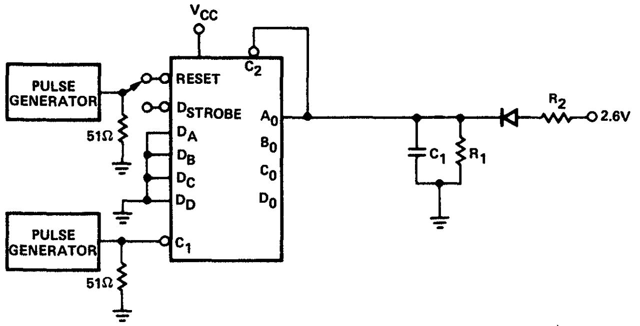


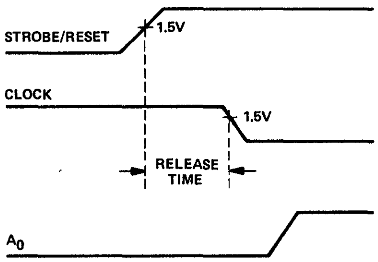




INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f = 5$ns max.
PRR = 40MHz, 50% duty cycle.

STROBE/RESET RELEASE TIME





NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, $V_{ac} = 25mV_{rms}$.
3. All diodes are 1N916.
4. R1 = 20k, R2 = 146Ω, C1 = 30pF.

PRESETTABLE LOW POWER DECADE/BINARY COUNTER

8292 8293

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8292 Decade Counter and 8293 Binary Counter are low power devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8292 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8293 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state, A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

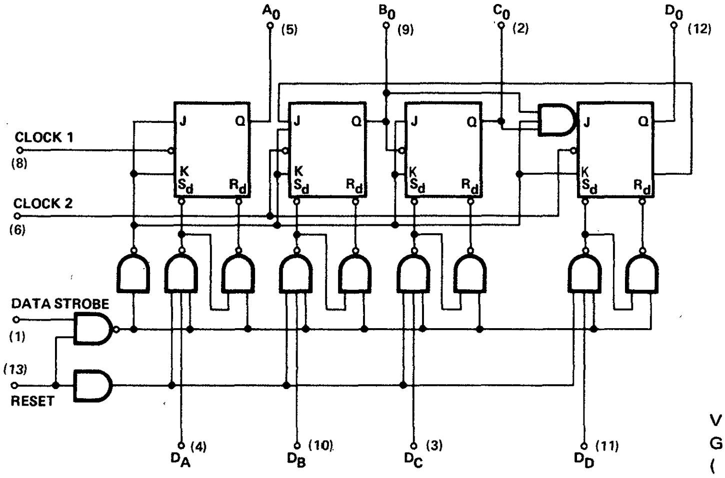
Triggering requirements are compatible with any of the 8000 Series elements.

The various counter arrangements, as well as additional applications suggestions may be found in the Signetics handbook "DESIGNING WITH MSI," Counters and Shift Registers,Volumn I.

LOGIC DIAGRAMS AND TRUTH TABLES

8292

Bi-Quinary (5-2)				
Input	B_0	C_0	D_0	A_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	1

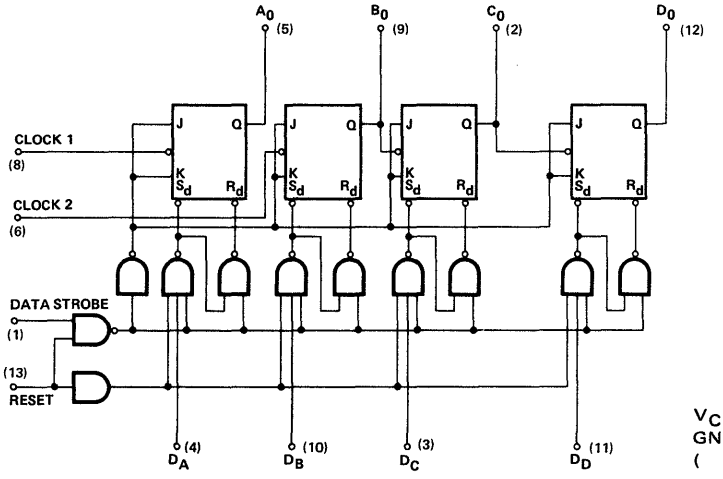


Decade (BCD)				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

8293

Binary				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V		A_{OUT}	-100μA	6,8
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V		A_{OUT}	3.2mA	6,9
"0" Input Current											
Data Strobe	-0.1		-0.4	mA	0.4V		5.25V				
Data Inputs	-0.1		-0.4	mA		0.4V					
Reset	-0.1		-0.6	mA	5.25V		0.4V				
Clock 1	-0.1		-0.6	mA	5.25V			0.4V			
Clock 2 (8292)	-0.1		-1.2	mA	5.25V				0.4V		
Clock 2 (8293)	-0.1		-0.6	mA	5.25V				0.4V		
"1" Input Current											
Data Strobe			20	μA	4.5V		0.0V				
Data Inputs			20	μA		4.5V					
Reset			40	μA	0.0V		4.5V				
Clock 1			40	μA	0.0V			4.5V			
Clock 2 (8292)			80	μA	0.0V				4.5V		
Clock 2 (8293)			40	μA	0.0V				4.5V		
Output Short Circuit Current	-5		-45	mA	0.0V					0.0V	7
Input Voltage Rating											
Data Strobe					10mA						
Clock 1 and 2	5.5			V				10mA	10mA		
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				

T_A = 25° C and V_{CC} = 5.0V

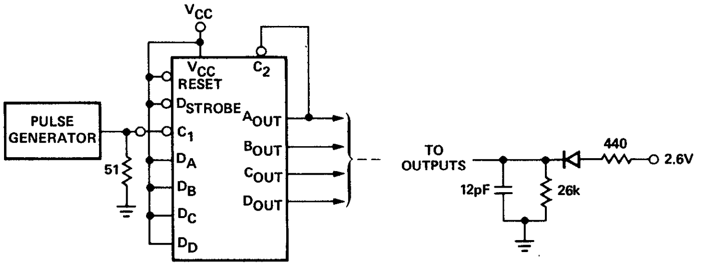
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Power/Current Consumption		52.5/ 10	69/ 13.1	mw/ mA			0.0V	0.0V	0.0V		13
Clock Mode t_{on} Delay (All Bits)		37	55	ns							10
Clock Mode t_{off} Delay (All Bits)		32	55	ns							10
Strobed Data t_{on} Delay (All Bits)		80	100	ns							10
Strobed Data t_{off} Delay (All Bits)		80	100	ns							10
Clock Mode Switching Test			75	ns							12
Strobe Pulse Width		60	75	ns		0.8V	2.0V	2.0V	A_{OUT}		
Reset Pulse Width		45	60	ns		2.0V	2.0V	2.0V	A_{OUT}		
Strobe/Reset Release Time		80		ns					A_{OUT}		
Toggle Rate	5	10		MHz							

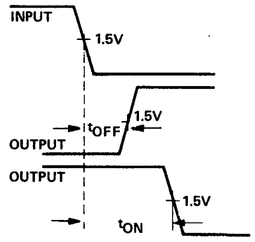
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Not more than one output should be shorted at a time.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Refer to AC Test Figure.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. This test guarantees the device will reliably trigger on a pulse with a 75ns fall-time or less.
13. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY



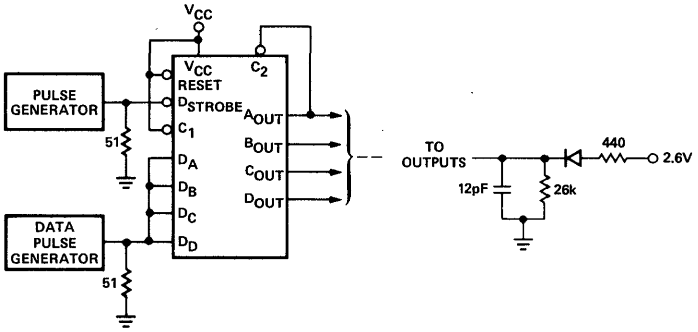


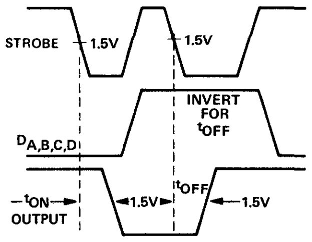
INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns, 50% to 50%
$t_r = t_f = 5ns$
PRR = 1MHz

NOTE:

1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.

STROBED DATA t_{on}/t_{off} DELAY



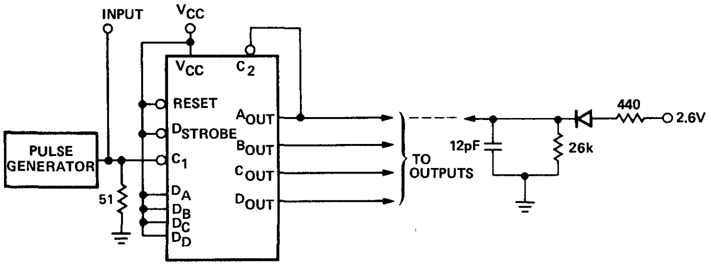


Strobe,
P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f = 5ns$

Data,
P.A. = 2.6V
P.W. = 500ns, 50% to 50%
PRR = 500KHz
$t_r = t_f = 5ns$

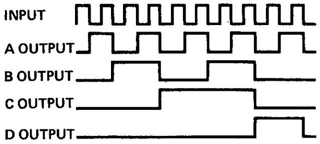
AC TEST FIGURES AND WAVEFORMS (Cont'd)

CLOCK MODE SWITCHING TEST

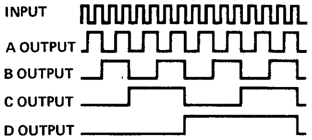


CIRCUIT UNDER TEST

8292

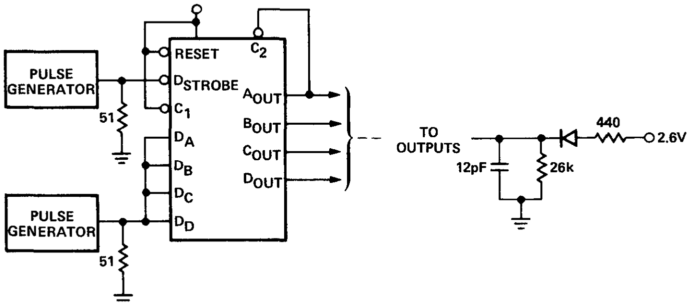


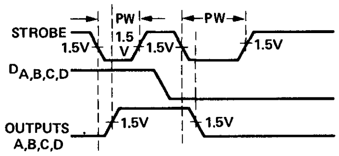
8293



INPUT PULSE:
Amplitude = 3.4V
P.W. = 100ns, 50% to 50%
PRR = 2.5MHz
t_r = 20ns
t_f = 75ns

MINIMUM STROBE PULSE WIDTH

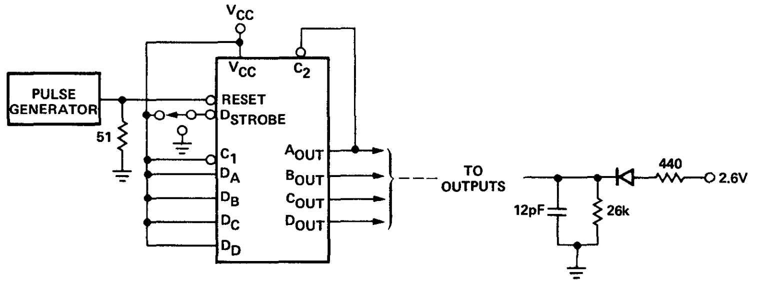


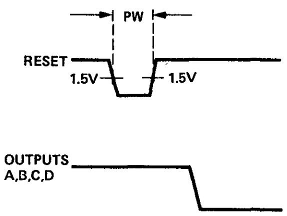


INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM RESET PULSE WIDTH

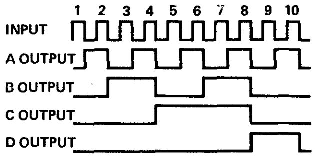


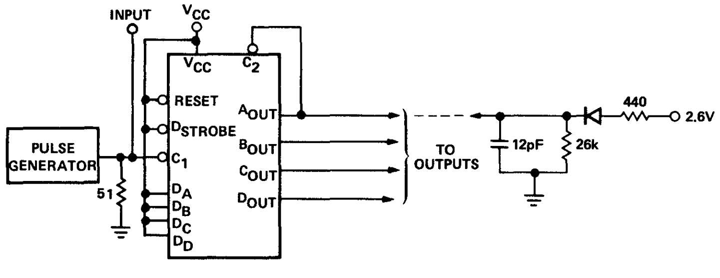


INPUT PULSE:
Amplitude 2.6V
$t_r = t_f$ = 5ns max.
NOTE: Outputs must be previously brought high by placing a "Q" on the D strobe input. A pulse generator may be substituted for the switch.

TOGGLE RATE

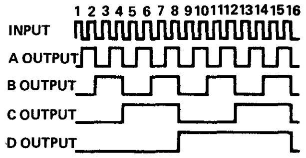
8292





CIRCUIT UNDER TEST

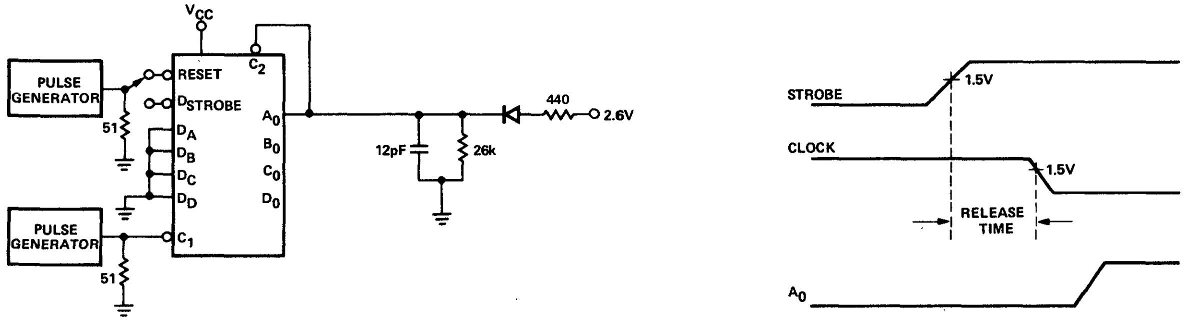
8293



INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

STROBE/RESET RELEASE TIME



CLOCK, STROBE/RESET:
Amplitude = 2.6V
PRR = 1MHz, 50% duty cycle
$t_r = t_f = 5ns$ max.

NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, f = 1MHz, $V_{ac} = 25mV_{rms}$.
3. All diodes are 1N916.

NIXIE DECODER/DRIVER 8T01

DIGITAL 8000 SERIES TTL/MSI

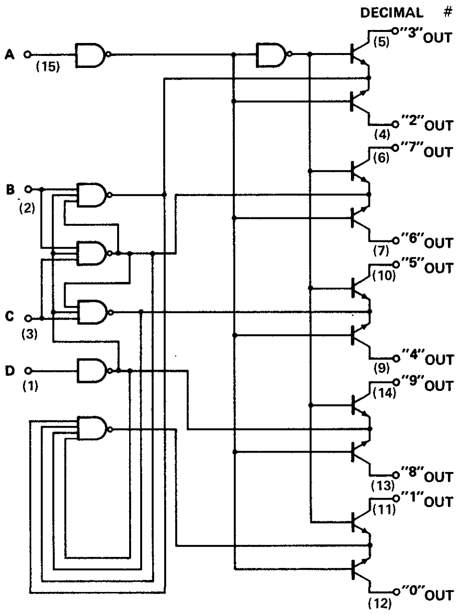
DESCRIPTION

The 8T01 Nixie* Decoder/Driver is a one-out-of-ten decoder which has been designed to provide the necessary high voltage characteristics required for driving gas-filled cold-cathode indicator tubes.

It may also be utilized in driving relays or other high voltage interface circuitry. The element is designed using TTL techniques and is therefore completely compatible with DTL and TTL elements.

The specially designed output drivers provide the necessary stable output state. There are no input codes where all outputs are "off" or where more than one output can be turned "on."

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	8
1	0	1	1	9
1	1	0	0	8
1	1	0	1	9
1	1	1	0	8
1	1	1	1	9

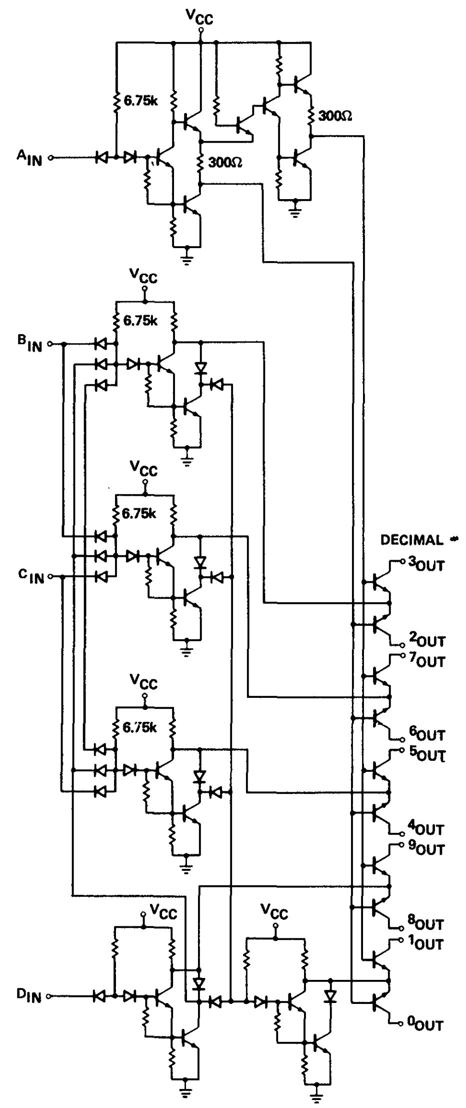
ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	
	MIN.	TYP.	MAX.	UNITS	INPUTS	OUTPUTS
"1" Output Voltage	68			V	0.8V	1.0mA
"0" Output Voltage			2.75	V	2.3V	5.0mA
"1" Input Current			40	μA	4.5V	
"0" Input Current (Aand D)			-0.9	mA	0.4V	
"0" Input Current (B and C)			-1.8	mA	0.4V	
Power Consumption		60		mW		

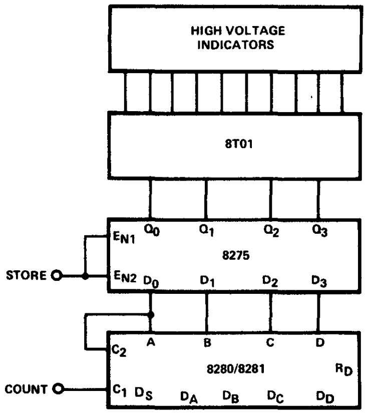
NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with Pin 8 tied to zero volts.
3. *Positive current flow is defined as into the terminal referenced.*
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN"Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process *changes and improvements.*
7. S8T01B operating temperature range is -20°C to +85°C.

SCHEMATIC DIAGRAM



TYPICAL APPLICATIONS



8T01 is used to decode output of 8280 or 8281 counter and drive NIXIE* indicator tubes.
An 8275 Quad-Latch is used as an intermediate storage register.

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*A trademark of the Burroughs Corporation.

SEVEN SEGMENT DECODER/DRIVER

8T04

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

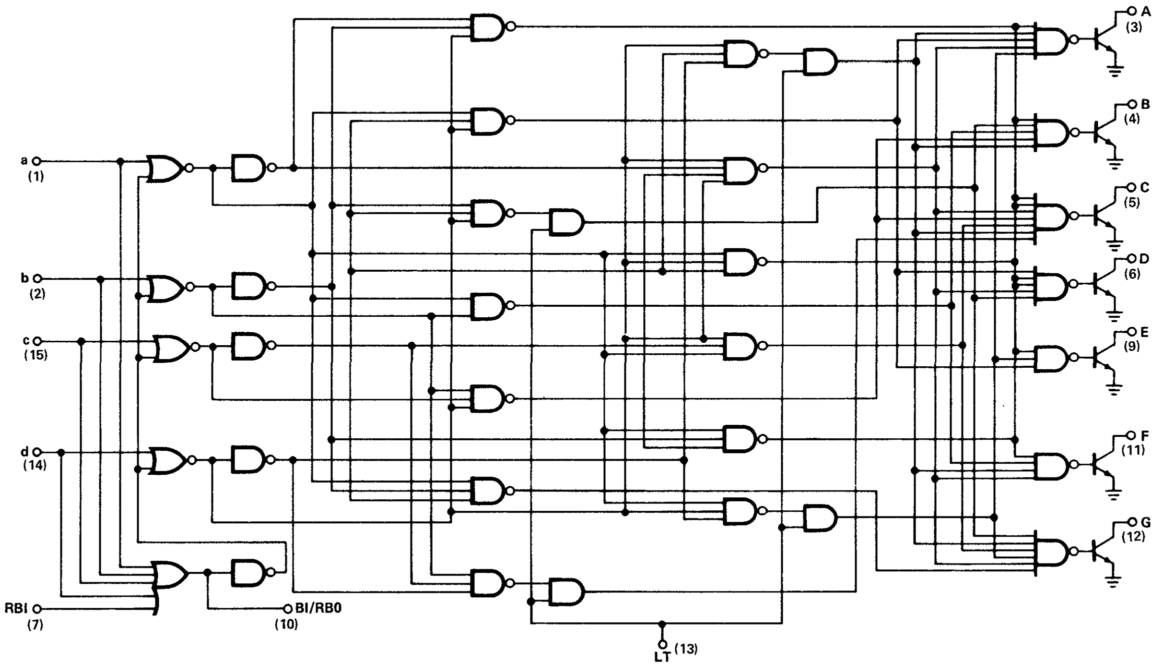
The 8T04 consists of the necessary logic to decode a 4-bit BCD code to seven segment (0 through 9) readout, as well as some selected signs and letters.

Incorporated in this device is a blanking circuit which turns all segments off when activated. The blanking circuit allows suppression of all numerically insignificant zeros, thereby presenting an easily read display.

Also included is the necessary circuitry to implement suppression of leading and/or trailing zeros. A Lamp Test control is provided to turn all segments on. The Lamp Test allows the viewer to check the validity of the display lamps.

High performance bare collector output transistors are used in the 8T04 for directly driving incandescent lamps or common anode LED displays.

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

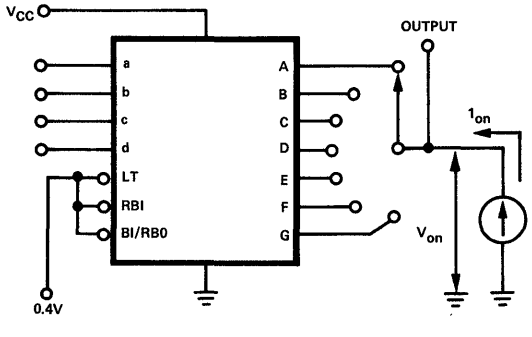
ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	LT	RB1	RBO B1	DRIVEN INPUTS	OUTPUTS	
"1" Output Voltage RBO	3.1			V			-160μA			7, 9
"0" Output Voltage										
RBO			0.4	V		0.8V	4.8mA	0.8V		8, 9
A-G			0.50	V	0.4V	0.4V	0.4V		40mA	8, 9
"1" Output Leakage Current (A-G)			100	μA		0.8V			6.0V	9, 10
"1" Input Current										
RBI			40	μA		4.5V				
LT			160	μA	4.5V					
All Other Inputs			80	μA		4.5V	4.5V	4.5V		
"0" Input Current										
RBI	-.1		-1.2	mA		0.4V				
BI	-.1		-2.2	mA			0.4V			
LT	-.1		-10	mA	0.4V					
All Other Inputs	-.1		-1.6	mA	0.4V			0.4V		
Input Latch Voltage	5.5			V			10mA			11
Power/Current Consumption:										
"S" Temperature Range			394/75	mW/mA						13
"N" Temperature Range			446/85	mW/mA						13

NOTES:

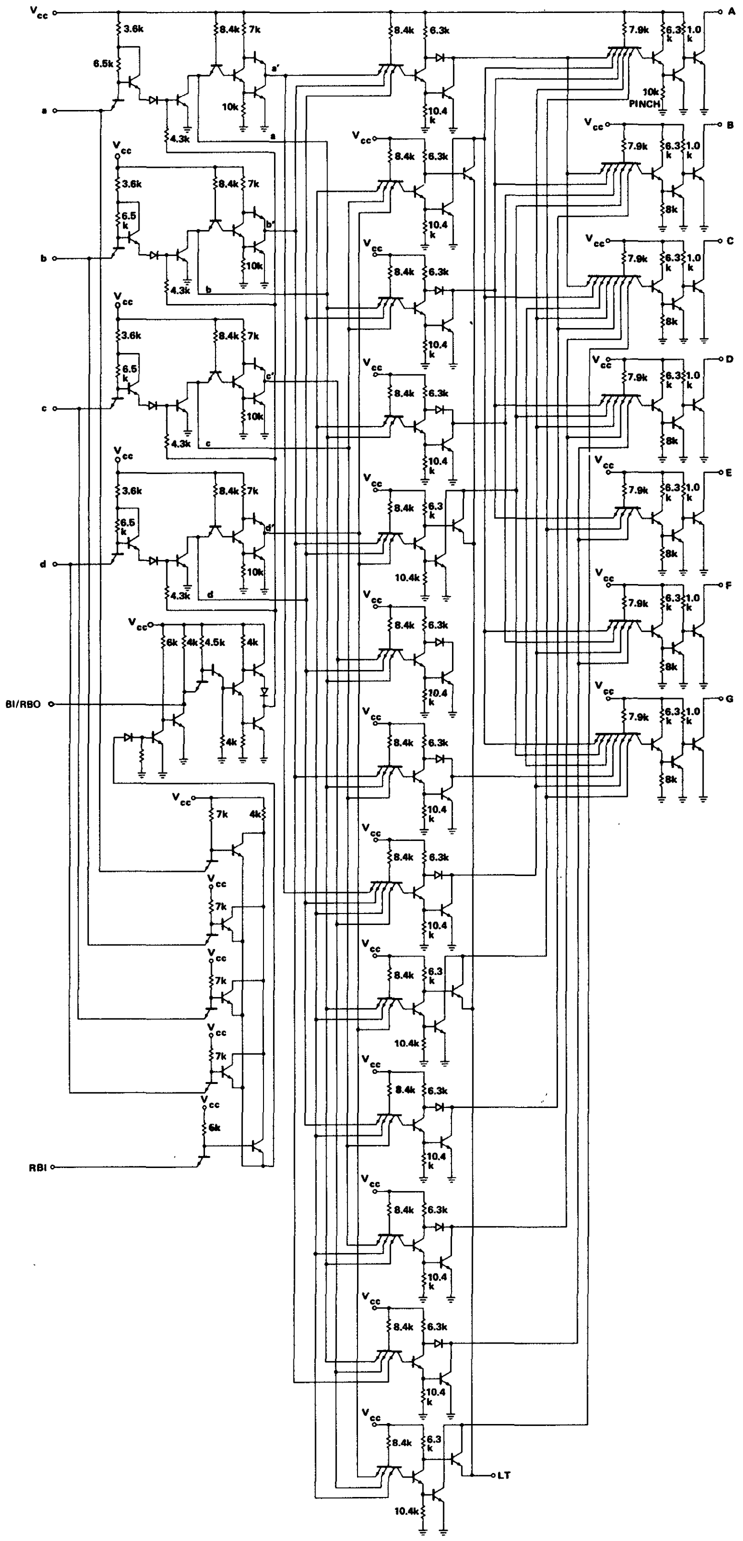
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
   "UP" Level = "1", "DOWN" = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. See truth table: "1" Threshold = 2.0V for a,b,c,d.
   "0" Threshold = 0.8V for a,b,c,d.
10. Connect an external 1k ±1% resistor to the output for this test.
11. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. V_{CC} = 5.25V.

TEST FIGURE FOR "0" OUTPUT VOLTAGE



Each output is tested separately in the ON state.

SCHEMATIC DIAGRAM



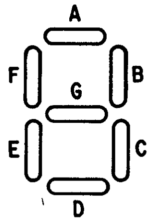
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							DISPLAY CHARACTER
d	c	b	a	LT		NOTE	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	0	0	0	0	0	0	0	8
X	X	X	X	1	X	0 (Note 1 & 2)	1	1	1	1	1	1	1	BLK
0	0	0	0	1	0	0 (Note 2)	1	1	1	1	1	1	1	BLK
0	0	0	0	1	1	1	0	0	0	0	0	0	1	0
0	0	0	1	1	X	1	1	0	0	1	1	1	1	1
0	0	1	0	1	X	1	0	0	1	0	0	1	0	2
0	0	1	1	1	X	1	0	0	0	0	1	1	0	3
0	1	0	0	1	X	1	1	0	0	1	1	0	0	4
0	1	0	1	1	X	1	0	1	0	0	1	0	0	5
0	1	1	0	1	X	1	1	1	0	0	0	0	0	6
0	1	1	1	1	X	1	0	0	0	1	1	1	1	7
1	0	0	0	1	X	1	0	0	0	0	0	0	0	8
1	0	0	1	1	X	1	0	0	0	1	1	0	0	9
1	0	1	0	1	X	1	1	1	1	1	1	1	0	—
1	0	1	1	1	X	1	1	1	1	1	1	1	1	BLK
1	1	0	0	1	X	1	0	0	0	1	0	0	0	A
1	1	0	1	1	X	1	1	1	0	1	1	1	1	,*
1	1	1	0	1	X	1	1	1	1	0	0	0	1	L
1	1	1	1	1	X	1	1	1	1	1	1	1	1	BLK

*COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.



SEVEN SEGMENT DECODER/TRANSISTOR DRIVER

8T05

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T05 consists of the necessary logic to decode a 4-Bit BCD code to seven segment (0 through 9) readout as well as some selected signs and letters.

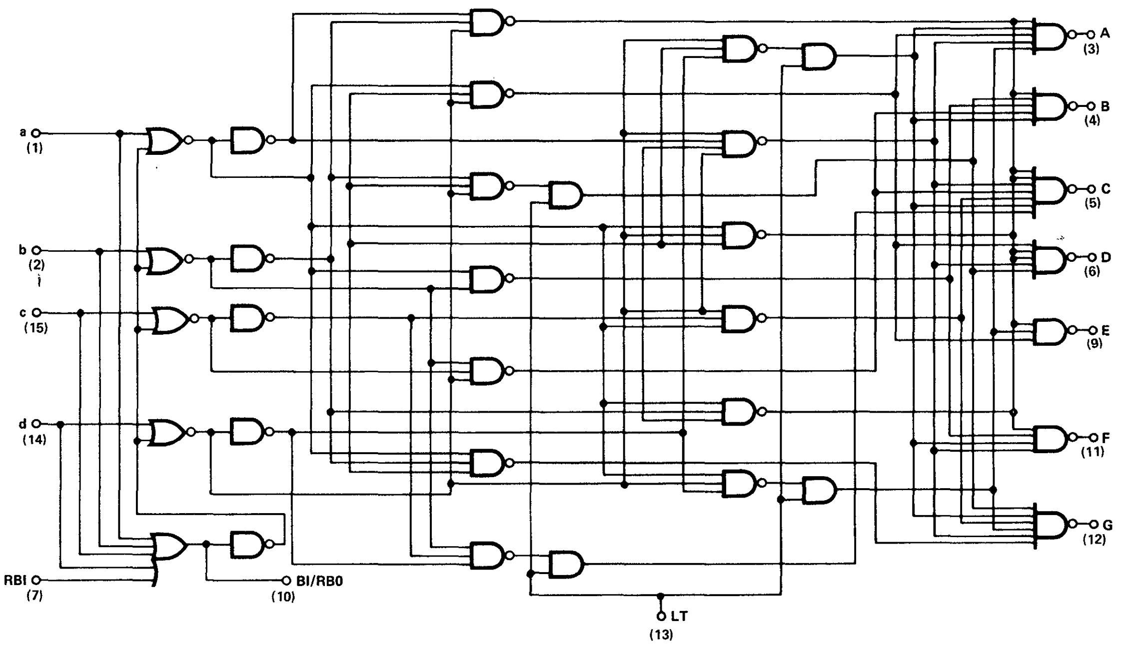
A Ripple Blanking input is provided to implement suppression of leading and/or trailing zeros. The suppression of all numerically insignificant zeros provides an easily read display.

Incorporated in the Ripple Blanking output (BI/RBO) is the facility to ground all the outputs. Blanking of the outputs allows for intensity modulation.

A Lamp Test input is provided which, when grounded forces all segment outputs high. This allows the viewer to check the validity of the display presentation by testing the integrity of the lamps.

The 8T05 has resistor pullups on the outputs to provide source current sufficient to drive interfacing elements. This allows the unit to drive high voltage transistors for neon displays. The 8T05 can also be used to drive common cathode LED displays at moderate light intensity levels.

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

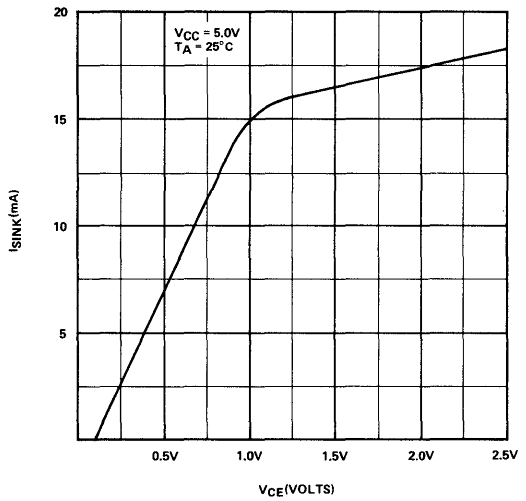
CHARACTERISTICS	LIMITS				LT	TEST CONDITIONS			OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS		RBI	RBO BI	DRIVEN INPUTS		
A-G "1" Output Voltage	3.9			V	0.4V				-500μA	7,9
A-G Output Source Current	-2.3			mA	0.4V				1.0V	
A-G "0" Output Voltage			0.3	V	4.5V	0.4V	0.4V		+500μA	8,9
RBO "1" Output Voltage	3.1			V			-160μA			7,9
RBO "0" Output Voltage			0.4	V		0.8V	4.8mA	0.8V		8,9
"1" Input Current										
RBI			40	μA		4.5V				
LT			160	μA	4.5V					
All other Inputs			80	μA		4.5V	4.5V	4.5V		
"0" Input Current										
RBI	-.1		-1.2	mA		0.4V				
BI	-.1		-2.2	mA			0.4V			
LT	-.1		-1.0	mA	0.4V					
All Other Inputs	-.1		-1.6	mA				0.4V		
Input Voltage Rating	5.5			V				10mA		10
Power/Current Consumption:										
"S" Temperature Range			394/75	mW/mA						12
"N" Temperature Range			110/85	mW/mA						12

NOTES:

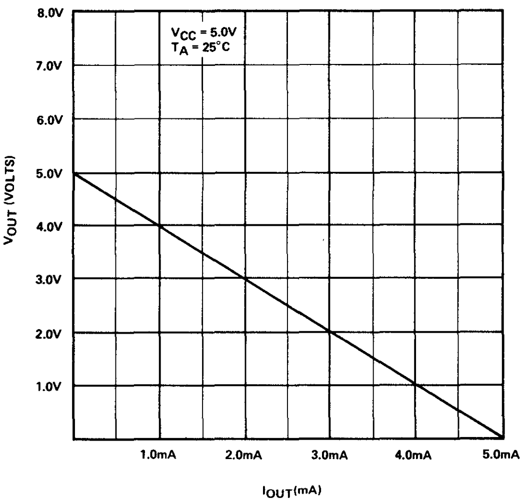
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. See truth table: "1" Threshold = 2.0V for a,b,c,d.
   "0" Threshold = 0.8V for a,b,c,d.
10. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. V_{CC} = 5.25V.

TYPICAL CHARACTERISTIC CURVES

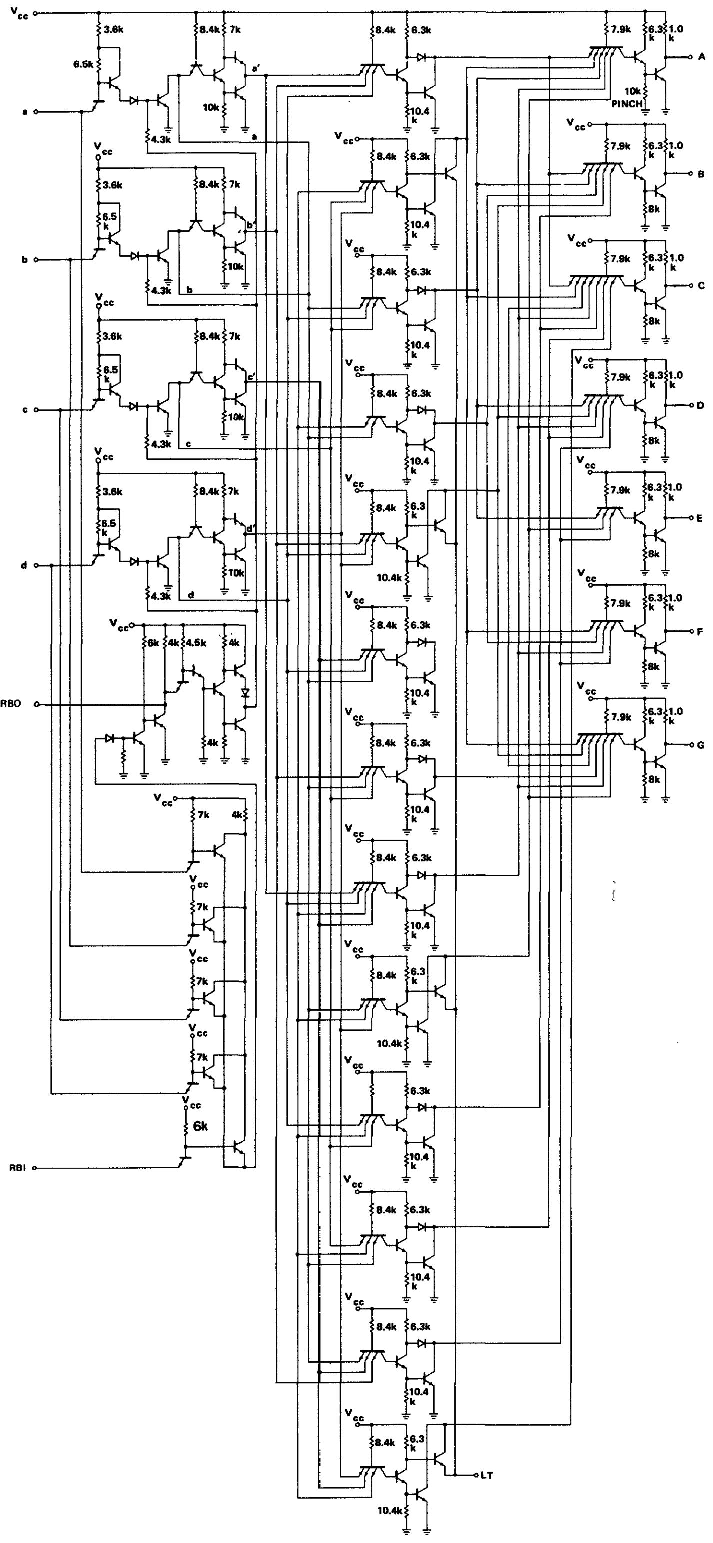
TYPICAL CURRENT SINK CAPABILITY VERSUS V_{CE}(SAT) (OUTPUTS A-G)



TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUTS A-G)



SCHEMATIC DIAGRAM



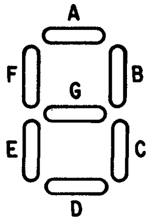
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							DISPLAY CHARACTER
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0 (Note 1 & 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 (Note 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	b
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	–
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	A
1	1	0	1	1	X	1	0	0	1	0	0	0	0	,*
1	1	1	0	1	X	1	0	0	0	1	1	1	0	L
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

*COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when a, b, c, d, RBI terminals are low, or damage may occur to the unit.



SEVEN SEGMENT DECODER/DISPLAY DRIVER

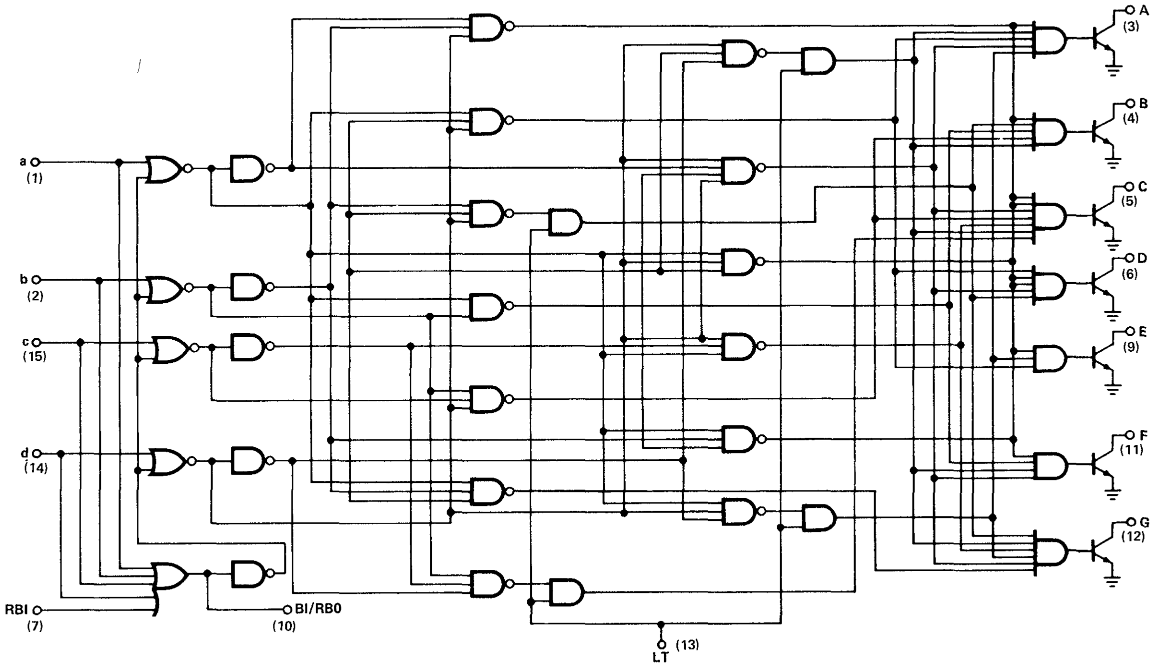
8T06

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T06 is a monolithic MSI circuit consisting of the necessary logic to decode a 4-bit BCD code to drive 7-segment indicators directly. Open-collector outputs are used for high current source applications, such as driving common cathode LED displays and discrete active components. The 8T06 seven segment decoder/driver accepts a 4-bit binary code and decodes all possible inputs as decimals 0-9 or selected signs and letters. Auxiliary inputs are provided for maximum versatility. The ripple blanking inputs (RBI) and the ripple blanking output (RBO) may be used for automatic leading and/or trailing-edge zero suppression. The RBO output also acts as an overriding blanking input (BI) which may be used for intensity modulation or strobing of the display. A lamp test (LT) input is provided to check the integrity of the display by activating all outputs independent of the input code.

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

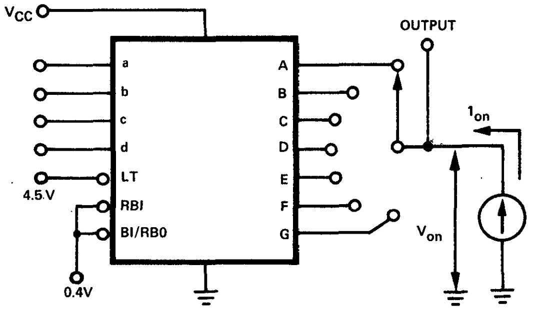
ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	LT	RB1	RBO B1	DRIVEN INPUTS	OUTPUTS	
"1" Output Voltage										
RBO	3.1			V			-160µA			7, 9
"0" Output Voltage										
(A-G)			0.5	V	4.5V	0.4V	0.4V		40mA	8, 9
RBO			0.4	V		0.8V	4.8mA	0.8V		8, 9
"1" Output Leakage Current										
(A-G)			100	µA	0.4V				6.0V	9, 10
"1" Input Current										
RBI			40	µA		4.5V				
LT			160	µA	4.5V					
All Other Inputs			80	µA		4.5V	4.5V	4.5V		
"0" Input Current										
RBI	-.1		-1.2	mA		0.4V				
BI	-.1		-2.2	mA			0.4V			
LT	-.1		-10	mA	0.4V					
All Other Inputs	-.1		-1.6	mA	0.4V	0.4V	0.4V	0.4V		
Input Voltage Rating	5.5			V		10mA		10mA		11
Power/Current Consumption:										11
"S" Temperature Range			394/75	mW/mA						13
"N" Temperature Range			446/85	mW/mA						13

NOTES:

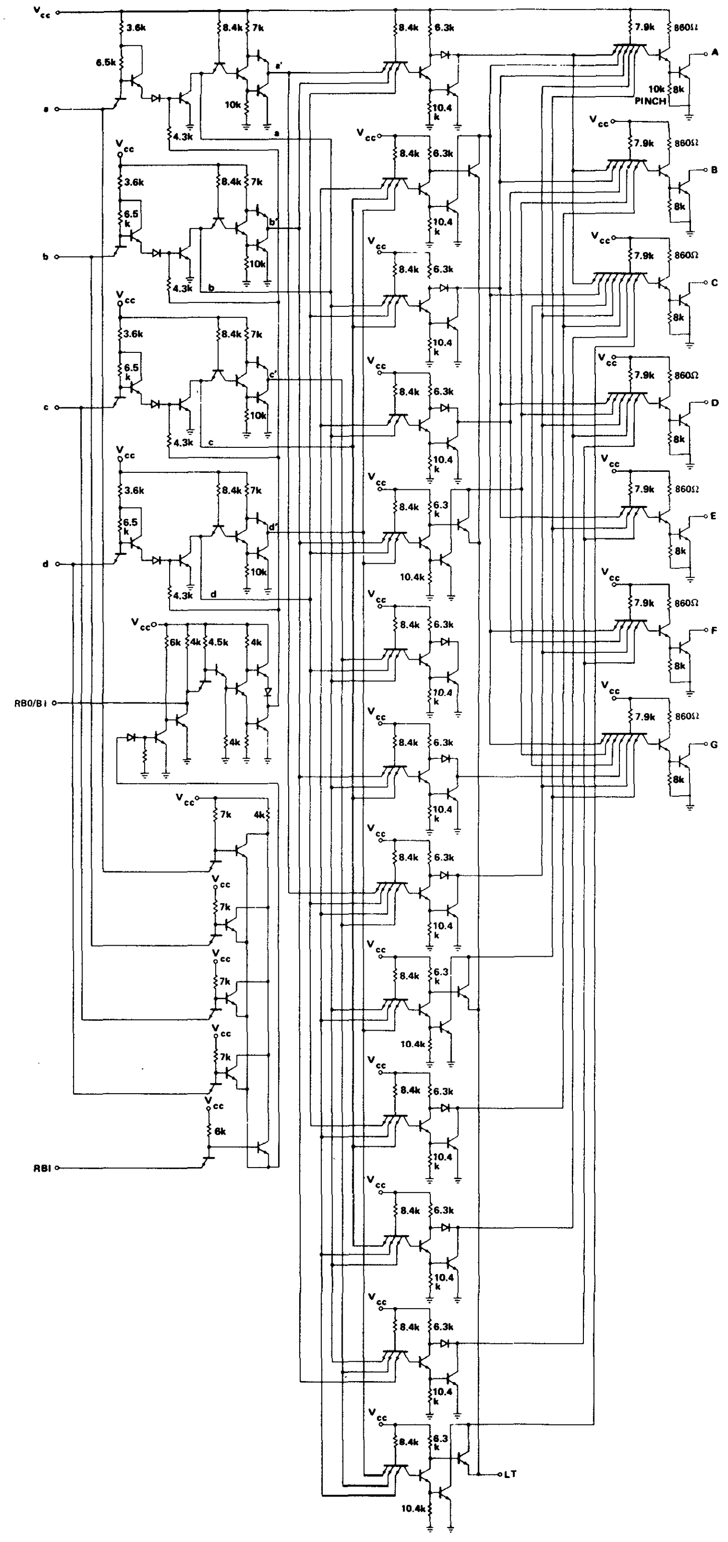
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definitions: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. See truth table: "1" Threshold = 2.0V for a,b,c,d. "0" Threshold = 0.8V for a,b,c,d.
10. Connect an external 1k ±1% resistor to the output for this test.
11. This test guarantees operation free of input latch-up over the specified operation supply voltage range.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. V_{CC} = 5.25 volts.

TEST FIGURE FOR "0" OUTPUT VOLTAGE



Each output is tested separately in the ON state.

SCHEMATIC DIAGRAM



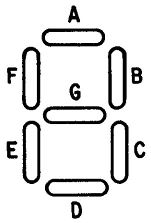
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							DISPLAY CHARACTER
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0 (Note 1 & 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 (Note 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	—
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	A
1	1	0	1	1	X	1	0	0	1	0	0	0	0	ı*
1	1	1	0	1	X	1	0	0	0	1	1	1	0	L
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

*COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when a, b, c, d, RBI terminals are low, or damage may occur to the unit.



QUAD BUS DRIVER 8T09

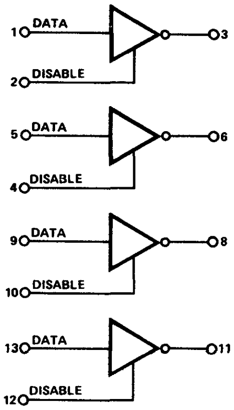
DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T09 is a high speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The outputs present a high impedance to the bus when disabled, (control input "1") and active drive when enabled (control input "0"). This eliminates the resistor pull-up requirement while providing performance superior to open collector schemes. Each output can sink 40mA and drive 300pF loading with guaranteed propagation delay less than 22 nanoseconds.

LOGIC DIAGRAM AND TRUTH TABLE

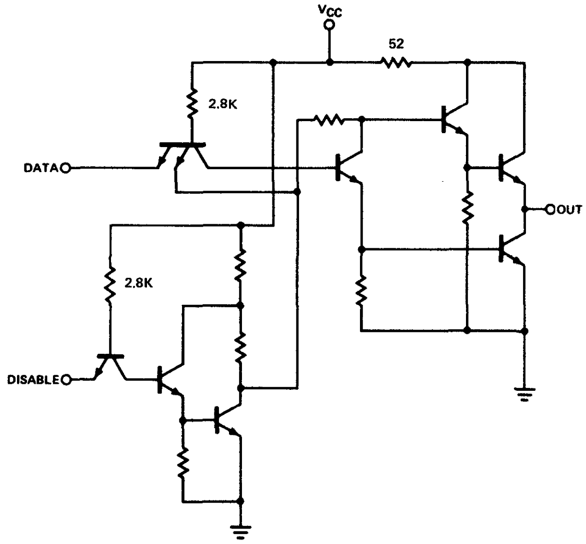


Data	Disable	Output
0	0	1
1	0	0
0	1	Hi- Z
1	1	Hi- Z

V_{CC} = (14)
GND = (7) A,F PACKAGES
( ) = Denotes Pin Numbers

V_{CC} = (4)
GND = (11) W PACKAGE

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA	DISABLE	OUTPUTS	
"1" Output Voltage	2.4	3.0		V	0.8V	0.8V	-5.2mA	7
"0" Output Voltage		0.2	0.4	V	2.0V	0.8V	40mA	8
Output Leakage Current	-40		+40	μA		2.0V	0.4V or 2.4V	3
"1" Input Current			40	μA		4.5V		
"0" Input Current			-2.0	mA	0.4V	0.4V		
Input Latch Voltage	5.5			V	10mA	10mA		
Power/Current Consumption		236/45	340/65	mW/mA				11
Output Short Circuit Current	-40		-120	mA	0V	0V	0V	

$T_A = 25°C$ and $V_{CC} = 5.0V$

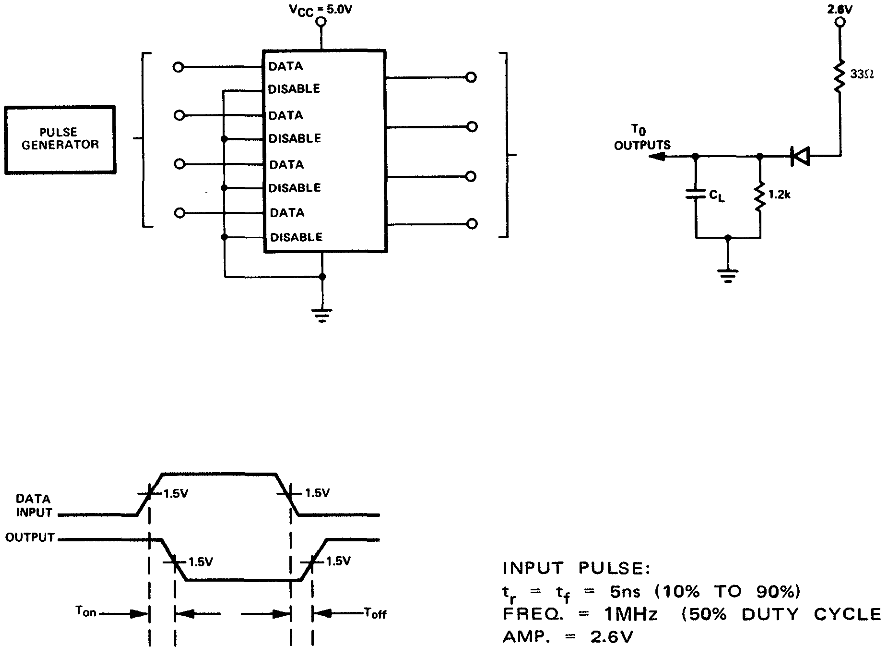
CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA	DISABLE	OUTPUTS	
Propagation Delay								
Data to Output								
t_{pd+}, t_{pd-}			10	ns			30pF load	9
			20	ns			300pF load	9
Disable to Output								
High Z to 0, 0 to High Z			14	ns			30pF load	9
			22	ns			300pF load	9
High Z to 1, 1 to High Z			14	ns			30pF load	9
			22	ns			300pF load	9

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

PROPAGATION DELAY (DATA TO OUTPUT)

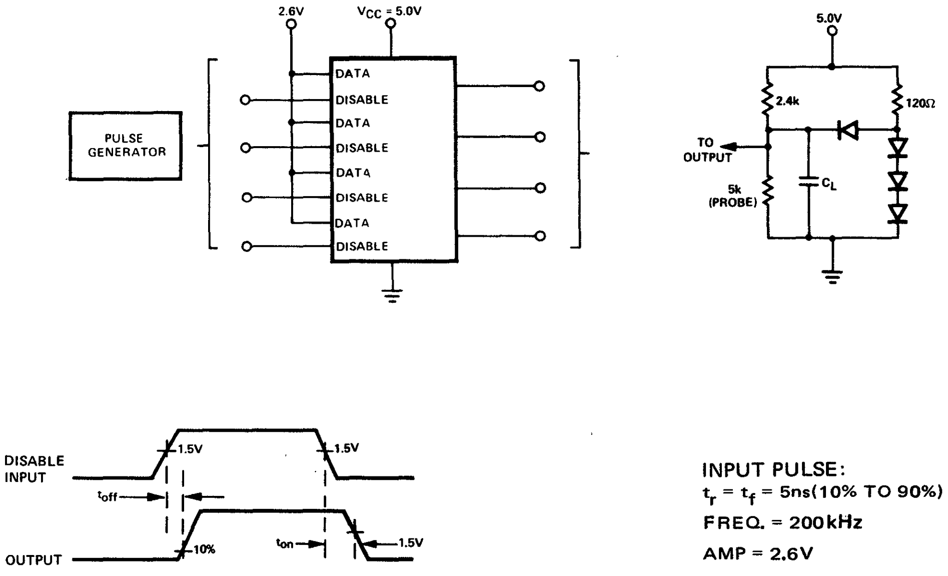


INPUT PULSE:
$t_r = t_f$ = 5ns (10% TO 90%)
FREQ. = 1MHz (50% DUTY CYCLE)
AMP. = 2.6V

FIGURE 1.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

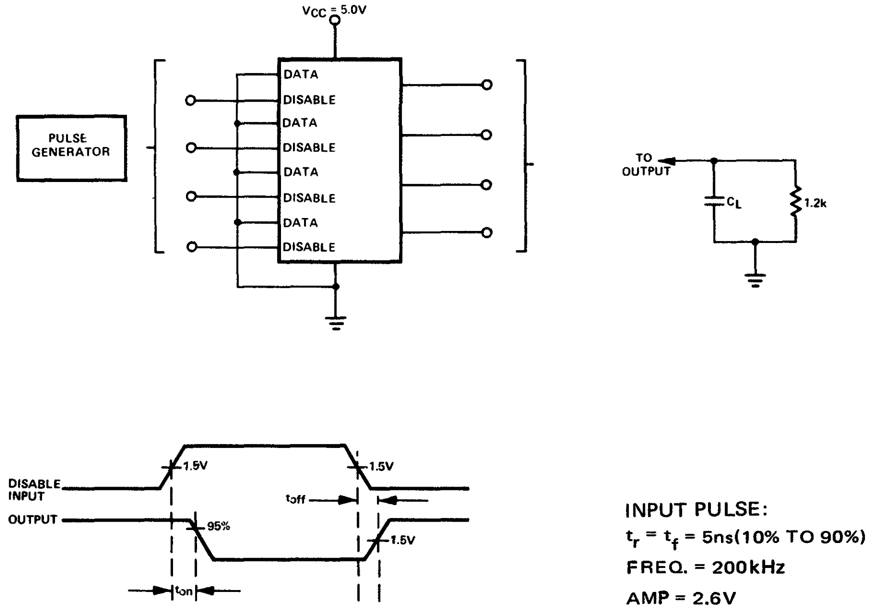
PROPAGATION DELAY ("0" TO HIGH Z)



INPUT PULSE:
$t_r = t_f$ = 5ns(10% TO 90%)
FREQ. = 200kHz
AMP = 2.6V

FIGURE 2.

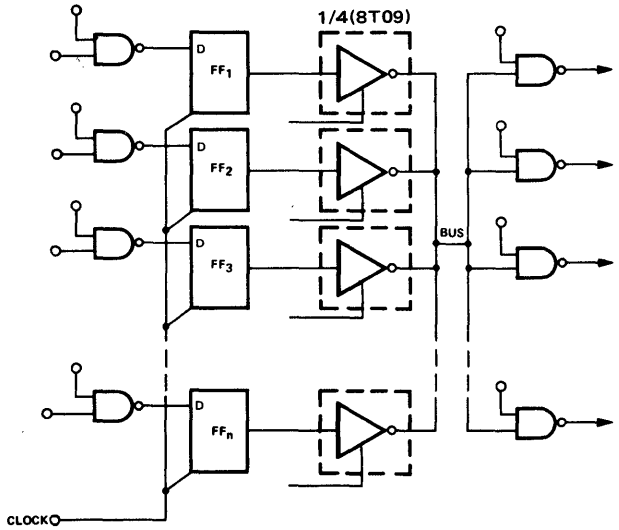
PROPAGATION DELAY ("1" TO HIGH Z)



INPUT PULSE:
$t_r = t_f$ = 5ns(10% TO 90%)
FREQ. = 200kHz
AMP = 2.6V

FIGURE 3.

TYPICAL APPLICATION



The above figure illustrates usage of the 8T09 in data processing logic. For example, FF_1 thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".

QUAD D-TYPE BUS FLIP-FLOP

8T10

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with a controlled impedance output for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A common clear input resets all flip-flops upon application of a logic "1" level.

Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

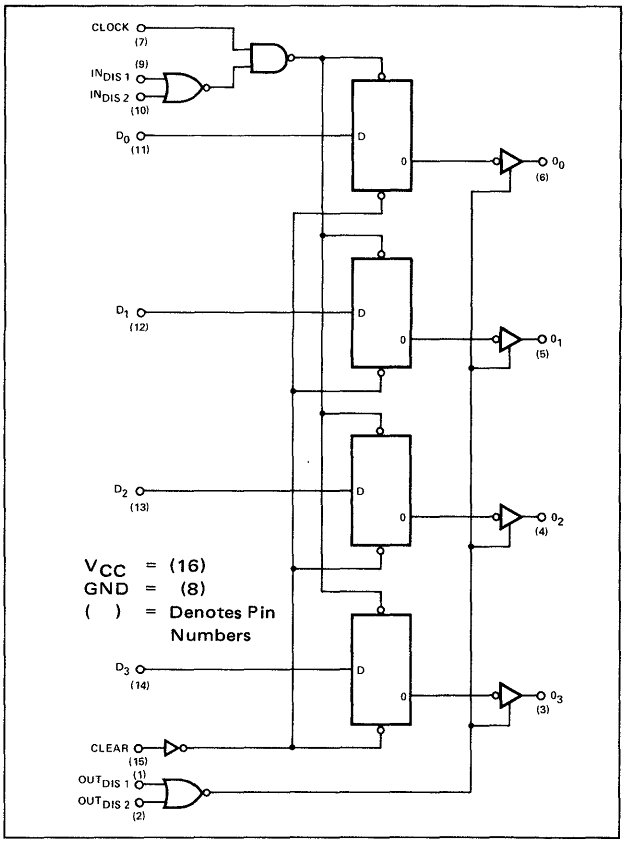
TRUTH TABLE

D_n	IN_{DIS}	OUT_{DIS}	0_{n+1}
0	0	0	0
1	0	0	1
X	1	0	0_n
X	X	1	High Z

0_n refers to the output state before a clock pulse.

$0_n + 1$ refers to the output state after a clock pulse.

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	IN DIS 1	IN DIS 2	OUT DIS 1	OUT DIS 2	CLEAR	CLOCK	OUTPUT	
"1" Output Voltage	2.4	3.0		V	2.0V	0.8V	0.8V	0.8V	0.8V	0.8V	Pulse	-5.2mA	6
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	Pulse	32mA	7
Output Leakage Current	-40		+40	µA		0.8	0.8V	+2.0V	+2.0V	0.8V	Pulse	+0.4V/ +2.4V	
(High Impedance State)													
"1" Input Current													
D_n Inputs			40	µA	4.5V	0.4V	0.4V	0.4V	0.4V	0.4V			
All Other Inputs			50	µA		4.5V	4.5V	4.5V	4.5V	4.5V	4.5V		
"0" Input Current													
D_n Inputs	-.100		-3.2	mA	0.4V								
All Other Inputs	-.100		-2.0	mA		0.4V	0.4V	0.4V	0.4V	0.4V	0.4V		
Input Latch Voltage	+5.5V				10mA	10mA	10mA	10mA	10mA	10mA	10mA		

$T_A = 25°C$ and $V_{CC} = 5.0V$

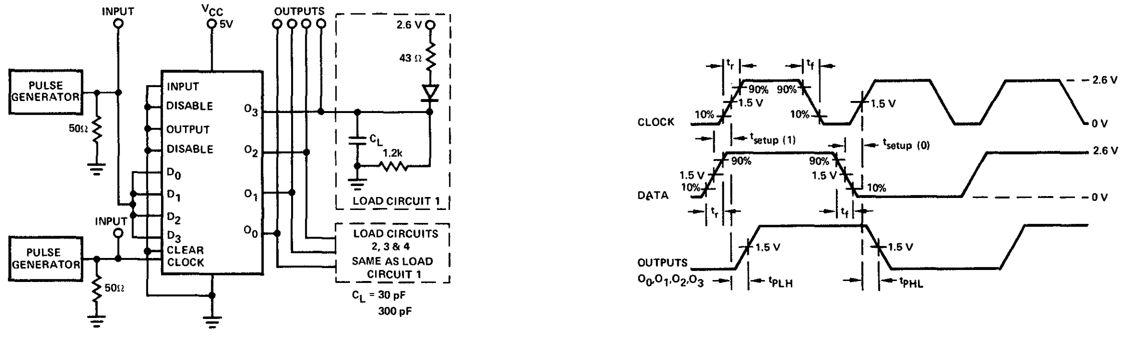
CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	IN DIS 1	IN DIS 2	OUT DIS 1	OUT DIS 2	CLEAR	CLOCK	OUTPUT	
Propagation Delay													
Clock to Output													
C_L = 30pf		18	25	ns									
C_L = 300pf		24	35	ns									
Disable to Output													
High Z to Logic 0 State (C_L = 300pf)		20	30	ns									10
Logic 0 State to High Z (C_L = 300pf)		20	30	ns									11
Clear to Output													
C_L = 30pf		15	22	ns									
C_L = 300pf		21	30	ns									
Set Up Time													
Data	+5	-1		ns									
Input Disable		−6	0	ns									
Hold Time													
Data		-1	+5	ns									
Reset Pulse Width	15			ns									
Clock Frequency	35	50		MHz									
Clock Pulse Width													
Positive		8	12	ns									
Negative		8	12	ns									
Power Supply Current			118	mA	0.4V	0.4V	0.4V	4.5V	0.4V	0.4V	4.5V		8
Output Short Circuit Current	-40		-120	mA	4.5V	0.4V	0.4V	0.4V	0.4V	0.4V		0.0V	

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. V_{CC} = 5.25V.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Measured to 1.5V level of output waveform.
11. Measured to 10% level of output waveform.
12. Refer to AC Test Circuits.

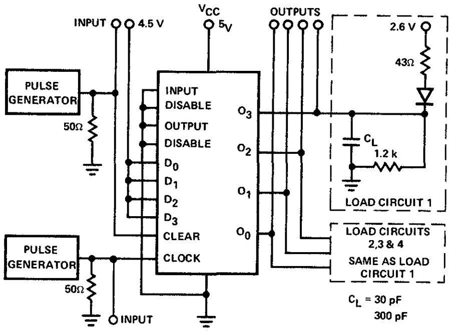
AC TEST CIRCUITS AND WAVEFORMS

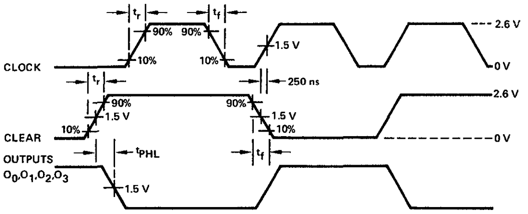
PROPAGATION DELAY (CLOCK TO OUTPUT)



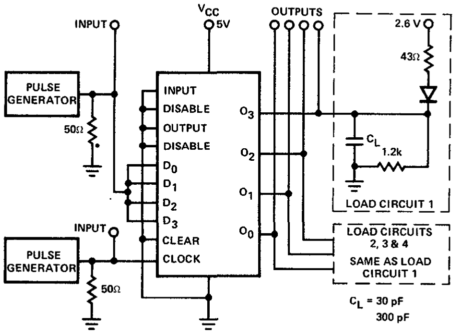
AC TEST CIRCUITS AND WAVEFORMS (Cont'd)

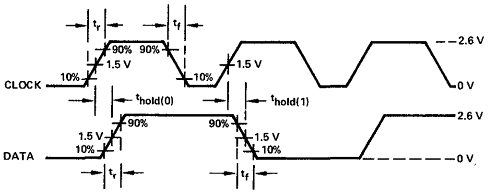
PROPAGATION DELAY (CLEAR TO OUTPUT)



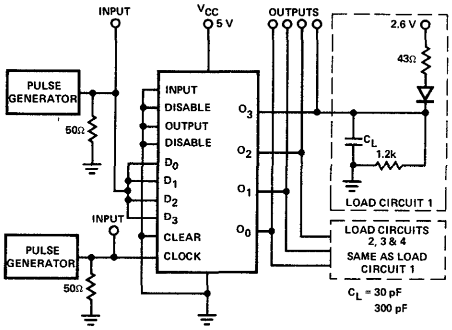


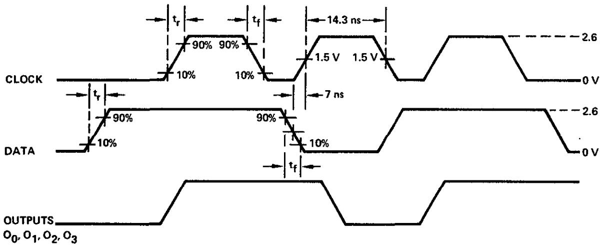
PROPAGATION DELAY (DATA HOLD TIME)



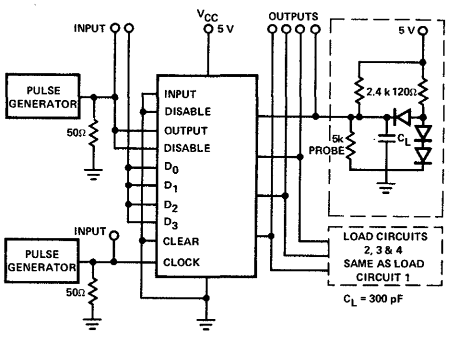


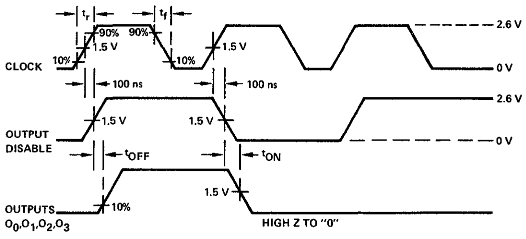
PROPAGATION DELAY (CLOCK FREQUENCY)



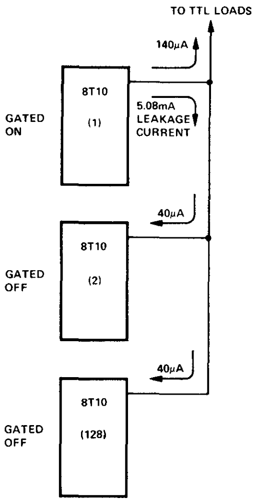


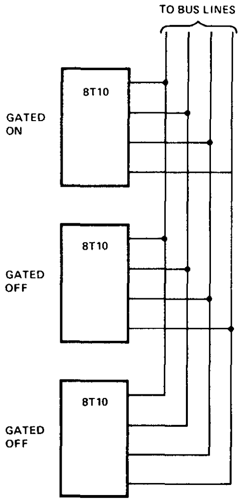
PROPAGATION DELAY (DISABLE TO OUTPUT)



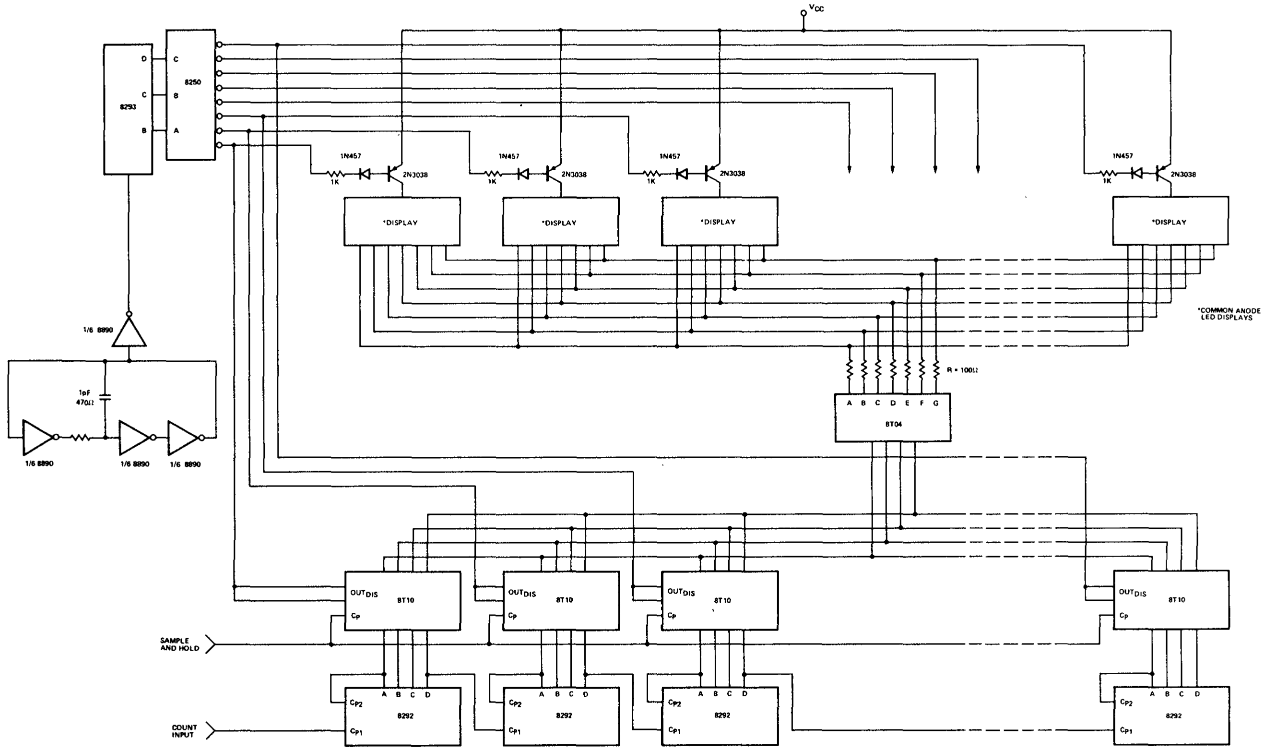


TYPICAL APPLICATIONS





MULTIPLEXING EIGHT LED DISPLAYS



DUAL LINE DRIVER 8T13

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T13 is a monolithic Dual Line Driver designed to drive 50 ohm or 75 ohm coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50Ω to 500Ω.

Key Design Benefits:

a. High-Power Drive Capability:
Specified at -75mA sink current rating at 2.4 volts (V "1" out) at 25°C.

b. Party-Line Operation:
Emitter-follower outputs enable two or more drivers to drive the same line. This permits multiple time-shared terminal connections since these drivers have no effect upon the transmission line unless activated.

c. Input gating structure allows employment of the "OR" as well as the "AND" function.

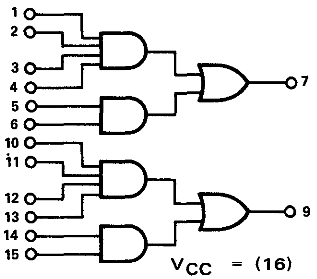
d. High Speed: $t_{on} = t_{off}$ = 20ns (max).

e. Input Clamp Diodes: Protects inputs from line ringing.

f. Single 5 Volt power supply.

g. Short Circuit Protection:
Incorporates a latch-back short circuit protection feature which protects the device by limiting the current it may source when operating under conditions of zero load resistance.

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE #1		INPUTS OF #2 AND GATE	OUTPUTS	
	MIN.	TYP.	MAX.	UNITS	INPUT UNDER TEST	OTHER INPUTS			
"1" Output Voltage	2.4			V	2.0V	2.0V	0.8V	-75mA	6
"1" Output Leakage Current			80	µA	0V	0V	0V	3.0V	7
"0" Output Leakage Current			-800	µA	0.8V	4.5V	0V	0.4V	
"0" Input Current	-0.1		-1.6	mA	0.4V	4.5V			
"1" Input Current			40	µA	4.5V	0V			

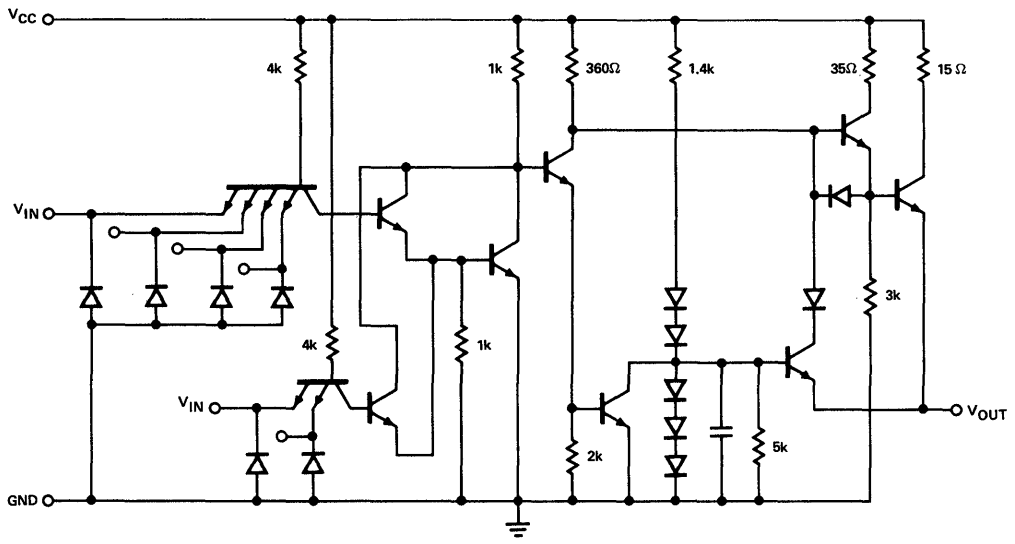
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS	
	MIN.	TYP.	MAX.	UNITS	INPUT UNDER TEST	OTHER INPUTS			
Turn-On Delay			20	ns					8.13
		32		ns					9.13
Turn-Off Delay			20	ns					8.13
		22		ns					9.13
Power/Current Consumption:									
Output at "0"			315/60	mW/mA	0.8V	0.8V	0.8V		12.15
Output at "1"			150/28	mW/mA	2.0V	2.0V	2.0V		12.15
Input Latch Voltage	5.5			V	10mA	0V	0V		11
"1" Output Current	-100		-250	mA	4.5V	4.5V	0V	2.0V	14
Output Short Circuit			-30	mA	4.5V	4.5V	0V	0V	14
Input Clamp Voltage			-1.5	V	-12mA				

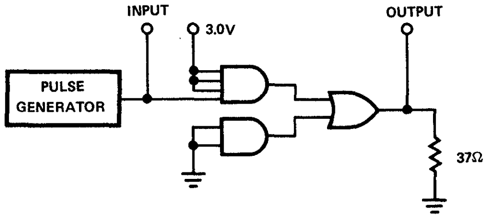
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. With forced output voltage of 3 volts no more than 500 μA will enter the driver when output is in "0" state. V_{CC} = 0V.
8. R_L = 37Ω to ground.
9. Load is 37Ω in parallel with 1000pF.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
12. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition.
13. Reference AC Test Figure and Pulse Requirements.
14. Reference "Typical Output Current vs Output Voltage Curve."
15. V_{CC} = 5.25 volts. Power Consumption specified for both drivers in package.

SCHEMATIC DIAGRAM

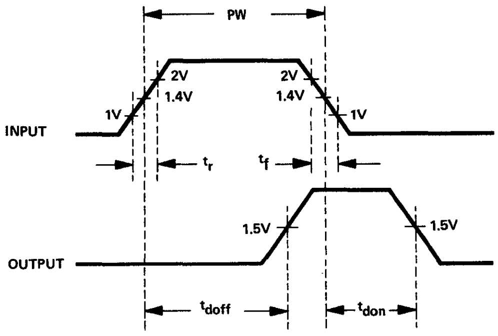


AC TEST FIGURE AND WAVEFORMS

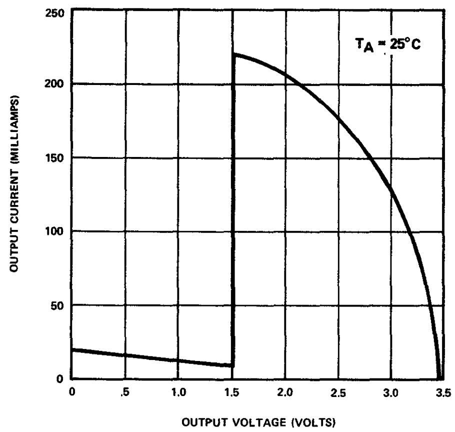


INPUT PULSE:
Amplitude = 3.0V
PW = 40ns (50% Duty Cycle)
t_r = t_f ≤5ns (10% and 90% measurement points)

PULSE REQUIREMENTS



TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE CURVE



TYPICAL APPLICATIONS

A typical application for the 8T13 is shown in Figure 1. If only one line driver is to be used for each transmission line, the line may be terminated with 50 ohms on the receiving end only. See Figure 2.

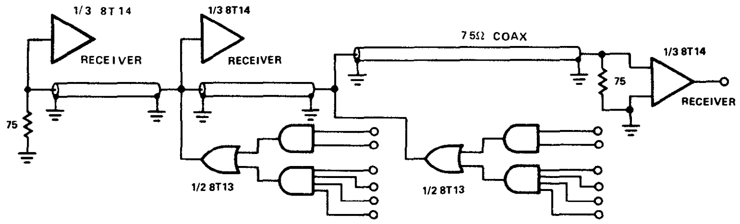


FIGURE 1

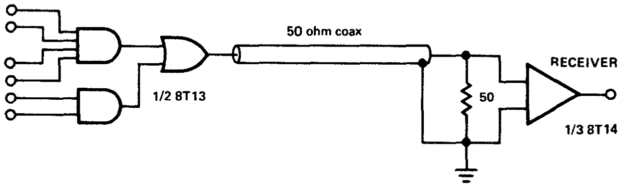


FIGURE 2

TRIPLE LINE RECEIVER

8T14

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T14 is a Triple Line Receiver designed for applications requiring digital information to be transmitted over long lengths of coaxial cable, strip line, or twisted pair transmission lines. The Receiver's high impedance input structure (≈30kΩ) presents a minimal load to the driver circuit and allows the transmission line to be terminated in its characteristic impedance to minimize line reflections.

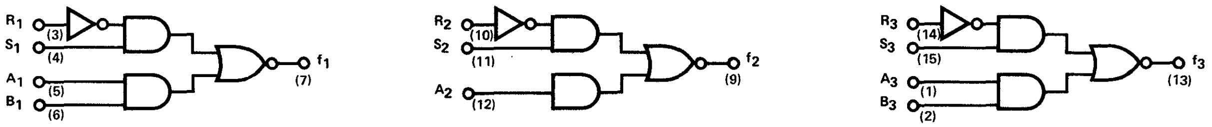
The built-in hysteresis characteristic of the 8T14 also makes it ideal for such applications as Schmitt triggers, one-shots and oscillators.

FEATURES

- BUILT-IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $t_{on} = t_{off} = 20\text{ns}$ (Typical)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5 VOLT LOGIC SUPPLY

*Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.5 volts typically and 0.3 volts minimum over the operating temperature range.

LOGIC DIAGRAMS



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	4.5V	0V	0V	-800µA	7, 13
	2.6	3.5		V	0V	0.8V	0V	0V	-800µA	7, 13
"0" Output Voltage			0.4	V	0.8V	2.0V	0V	0V	16mA	8, 12
			0.4	V	0V	0V	2.0V	2.0V	16mA	8, 12
"0" Input Current:										
S_n	-0.1		-1.6	mA	0V	0.4V				
A_n	-0.1		-1.6	mA	0V		0.4V			
B_n	-0.1		-1.6	mA				0.4V		
"1" Input Current										
R_n			0.17	mA	3.8V					
S_n			40	µA	3.8V	4.5V				
A_n			40	µA			4.5V	0V		
B_n			40	µA			0V	4.5V		
Hysteresis	0.30	0.50		V		4.5V	0V	0V		10, 11

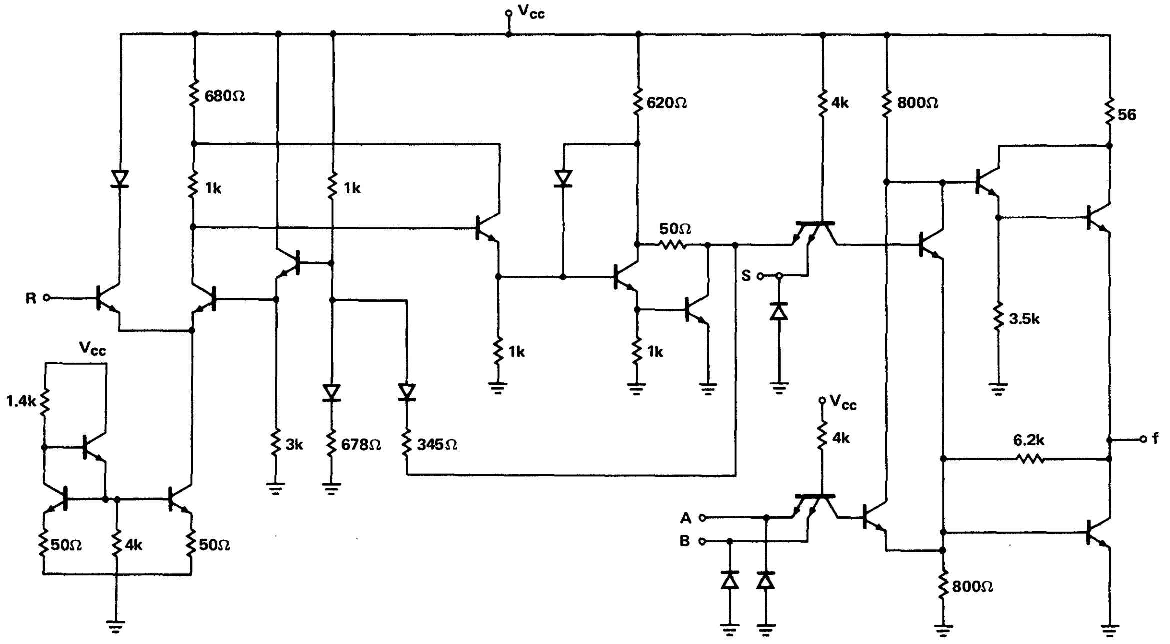
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
Turn-On Propagation Delay		20	30	ns						
Turn-Off Propagation Delay		20	30	ns						
Power/Current Consumption		315/60	380/72	mW/mA						
Input Voltage Rating										
S	5.5			V	3.8V	10mA	0V	0V		
A	5.5			V	0V	0V	10mA	0V		
B	5.5			V	0V	0V	0V	10mA		
Output Short Circuit Current	-50		-100	mA	3.8V	0V	0V	0V	0V	
Input Clamp Voltage:										
S			-1.5	V		-12mA				
A			-1.5	V			-12mA			
B			-1.5	V				-12mA		

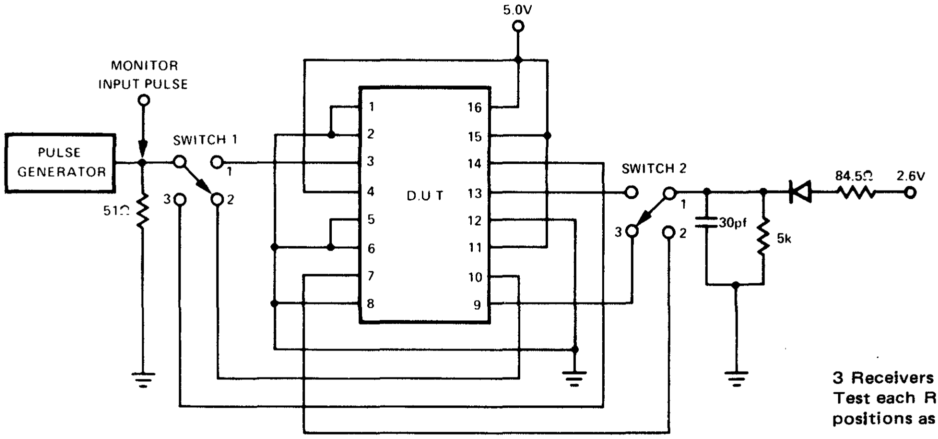
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
3. Positive current flow is defined as into the terminal referenced.
4. Positive Logic Definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
10. Hysteresis is defined as voltage difference between R input level at which output begins to go from "0" to "1" state and level at which output begins to go from "1" to "0".
11. $V_{CC} = 5.0V$.
12. Previous condition is a "1" output state.
13. Previous condition is a "0" output state.
14. $V_{CC} = 5.25$ volts.

SCHEMATIC DIAGRAM

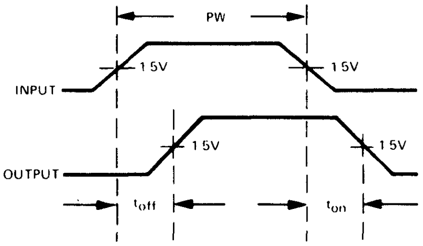


AC TEST CIRCUIT AND WAVEFORMS



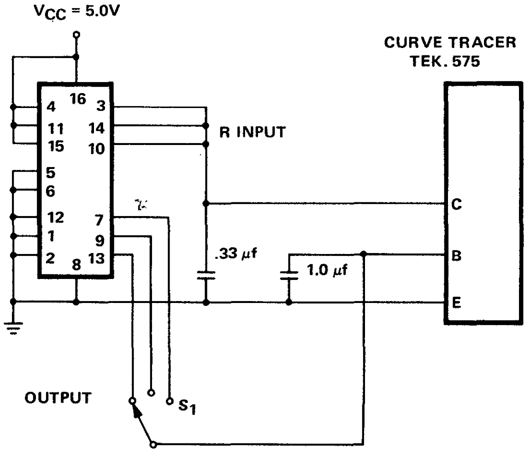
3 Receivers in the package.
Test each Receiver using switch positions as shown in Table I.

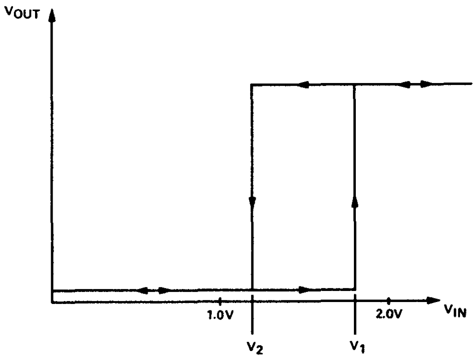
TABLE I		
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3



Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

HYSTERESIS TEST CIRCUIT





Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.8V minimum and 2.0V max.
2. Hysteresis = $V_1 - V_2 \geqslant 0.3$V.

FIGURE 1

FIGURE 2

TYPICAL APPLICATIONS

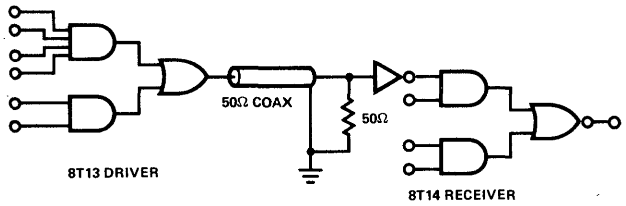
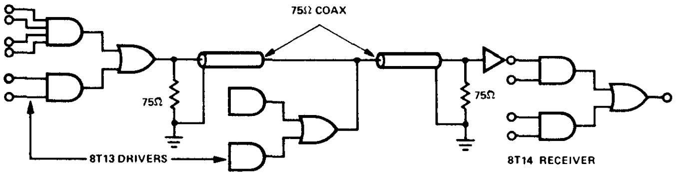


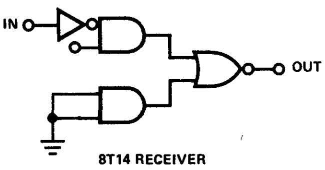
FIGURE 1

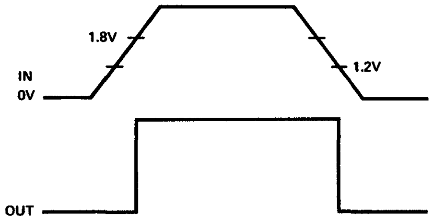


If more than one driver/receiver is to be used for each transmission line, the line should be terminated at both ends as shown in Fig. 2.

FIGURE 2

SCHMITT TRIGGER APPLICATION





DUAL COMMUNICATIONS EIA/MIL LINE DRIVER

8T15

PRODUCT AVAILABLE IN 0°C TO +75°C TEMPERATURE RANGE ONLY

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T15 Dual Communications Line Driver provides line driving capability for data transmission between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V 24.

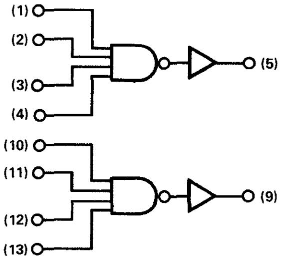
This dual 4-input NAND driver will accept standard TTL logic level inputs and will drive interface lines with nominal data levels of +6V and -6V. Output slew rate may be adjusted by attaching an external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as ±25V.

ABSOLUTE MAXIMUM RATINGS*

Input Voltage	+5.5V
Output Voltage	±25V
V_{CC}	+15V
V_{EE}	−15V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C

*Limiting values above which serviceability may be impaired.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS		OUTPUTS	
					DRIVEN	OTHER		
"1" Output Voltage	+5.0	+6.0	+7.0	V	0.8V		-4.0mA	
"0" Output Voltage	-5.0	-6.0	-7.0	V	2.0V		4.0mA	
"0" Input Current	-0.1	-0.8	-1.6	mA	0.4V			
"1" Input Current			40	μA	4.5V	0.0V		

SIGNETICS DIGITAL 8000 SERIES TTL/MSI – 8T15

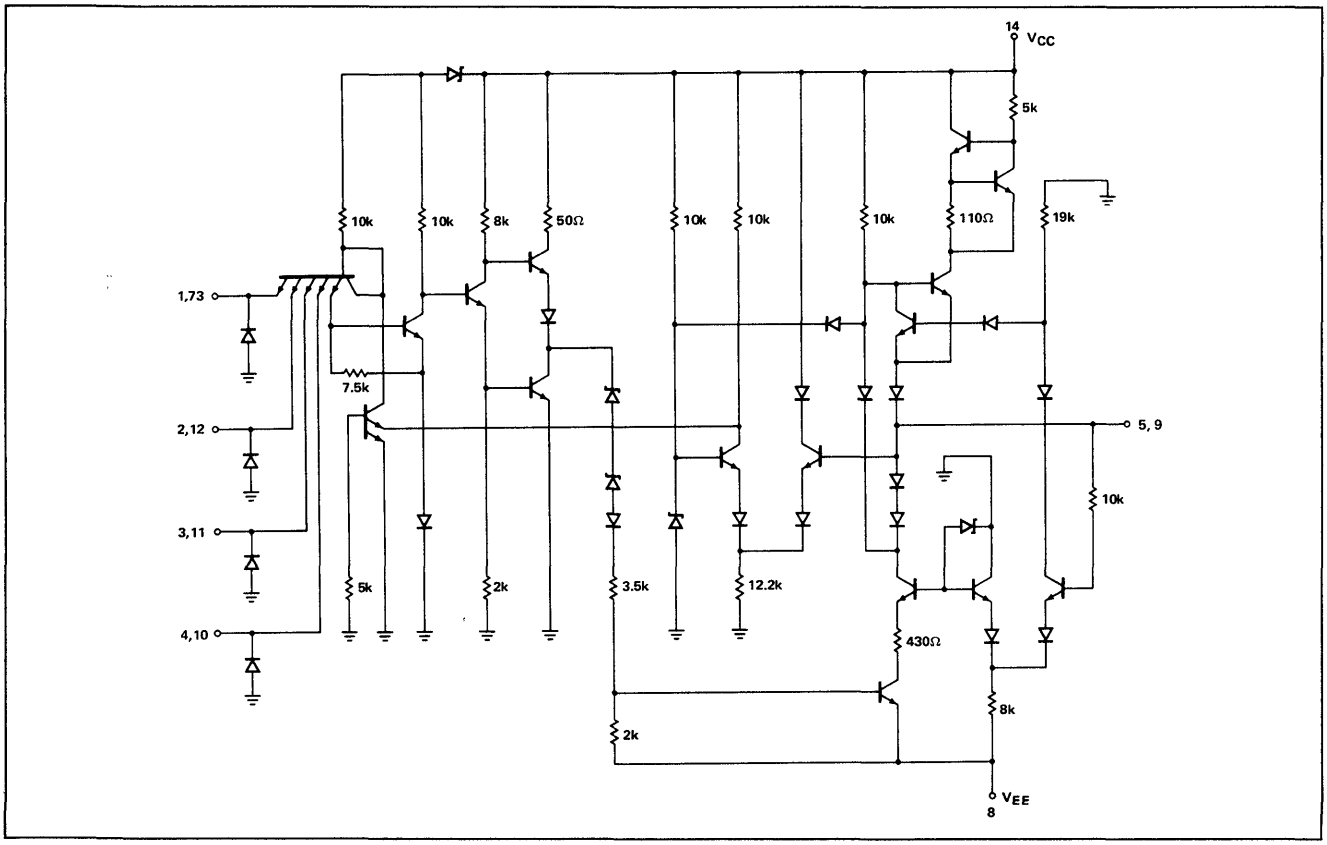
$T_A = 25^oC$, $V_{CC} = +12.0V$, $V_{EE} = -12.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS DRIVEN	INPUTS OTHER	OUTPUTS	
Output Rise Time			4	µs			Load A	8
Output Fall Time			4	µs			Load B	8
Output Rise Time	200			ns			Load C	8
Output Fall Time	200			ns			Load D	8
Power Consumption (per driver)			275	mW				10
Current from Positive Supply			16	mA				10
Current from Negative Supply			28	mA				10
Input Latch Voltage Rating	5.5			V	10mA	0.0V		7
Output Short Circuit Current			-25	mA	0.0V		-25V	9, 10
			+25	mA			+25V	9, 10
Output Impedance								
(Power on)		95		ohms	0.0V		-3.5±1mA	
(Power on)		95		ohms	0.0V		+3.5±1mA	
(Power off)	300	2.5M		ohms			±2V	
Input Clamp Voltage			-1.5	V	-12.0mA			

NOTES:

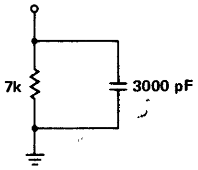
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
8. Rise and fall times are measured between the +3V and -3V points on the output waveform.
9. Test each driver separately.
10. $V_{CC} = +12.6V$, $V_{EE} = -12.6V$

SCHEMATIC DIAGRAM

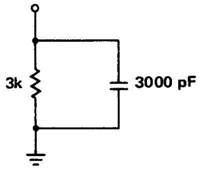


AC TEST FIGURES & WAVEFORMS

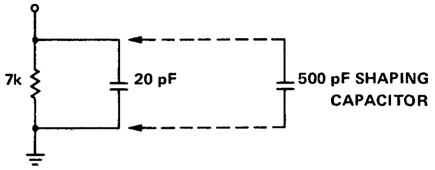
LOAD A



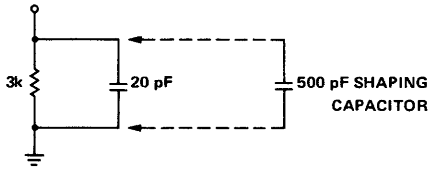
LOAD B

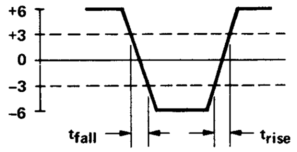


LOAD C

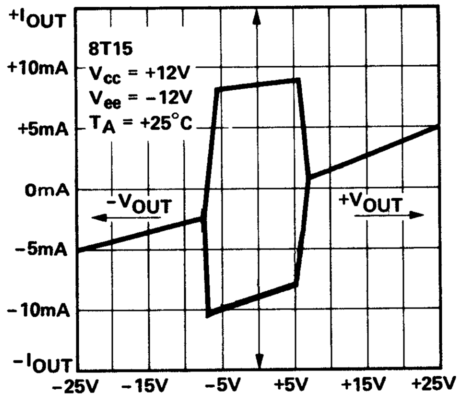


LOAD D



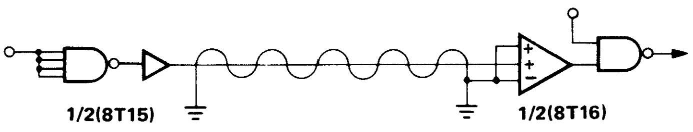


TYPICAL OUTPUT CHARACTERISTIC CURVE

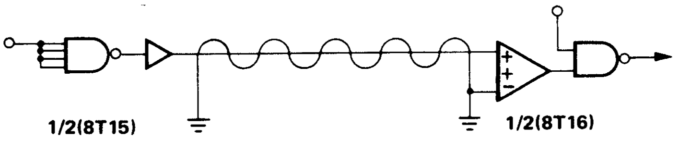


TYPICAL APPLICATIONS

HIGH DIFFERENTIAL NOISE IMMUNITY (EIA + INPUT)



HIGH COMMON MODE NOISE IMMUNITY (MIL + INPUT)



DUAL COMMUNICATIONS EIA/MIL LINE RECEIVER 8T16

PRODUCT AVAILABLE IN 0° TO +75°C TEMP. RANGE ONLY.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T16 Dual Communications Line Receiver provides receiving capability for data lines between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL-STD-188B and CCITT V24.

The receivers accept single (EIA) or double ended (MIL) inputs and are provided with an output strobing control. Both EIA and MIL input standards are accommodated.

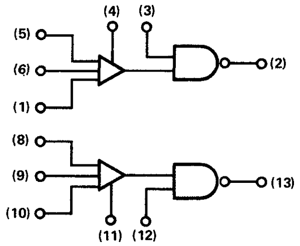
When using the EIA input terminal (with the Hysteresis terminal open), input voltage threshold levels are typically +2V and -2V with a guaranteed minimum Hysteresis of 2.4V. By grounding the "Hysteresis" terminal, the EIA input voltage threshold levels may be shifted to typically +1.0V and +2.1V with a minimum guaranteed Hysteresis of 0.75V. (Note that when using the EIA inputs, the MIL inputs—both positive and negative—must be grounded).

The MIL input voltage threshold levels are typically +0.6V and —0.6V with a minimum guaranteed Hysteresis of 0.7V. A MIL negative terminal is provided on each receiver per specification MIL-STD-188B to provide for common mode noise rejection.

Each receiver includes a strobe input so that:

a. A "1" on the strobe input allows data transfer.
b. A "0" on the strobe input holds the output high.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ABSOLUTE MAXIMUM RATINGS*

Input Voltage (EIA and MIL)	±25V
V_{CC}	+7.0V
Storage Temperature	-65°C to +175°C
Operating Temperature	0°C to +75°C

*Limiting values above which serviceability may be impaired.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						
					INPUTS					OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS	EIA	MIL(+)	MIL(-)	HYS	STROBE		
"1" Output Voltage (EIA) ("Hysteresis" Open)	2.6	3.5		V	-3.0V	0V	0V		2.0V	-800μA	8, 12
"1" Output Voltage (EIA) ("Hysteresis" grounded)	2.6	3.5		V	+0.3V	0V	0V	0V	2.0V	-800μA	8, 10
"1" Output Voltage (MIL)	2.6	3.5		V		-0.1mA	0V		2.0V	-800μA	8, 11
	2.6	3.5		V		-0.9V	0V		2.0V	-800μA	8, 11
"1" Output Voltage (Strobe)	2.6	3.5		V	+3.0V	0V	0V		0.8V	-800μA	8
"0" Output Voltage (EIA) ("Hysteresis" Open)			0.4	V	+3.0V	0V	0V		2.0V	9.6mA	9, 12
"0" Output Voltage (EIA) ("Hysteresis" grounded)			0.4	V	+3.0V	0V	0V	0V	2.0V	9.6mA	9, 12
"0" Output Voltage (MIL)			0.4	V		+0.1mA	0V		2.0V	9.6mA	9, 13
			0.4	V		+0.9V	0V		2.0V	9.6mA	9, 13

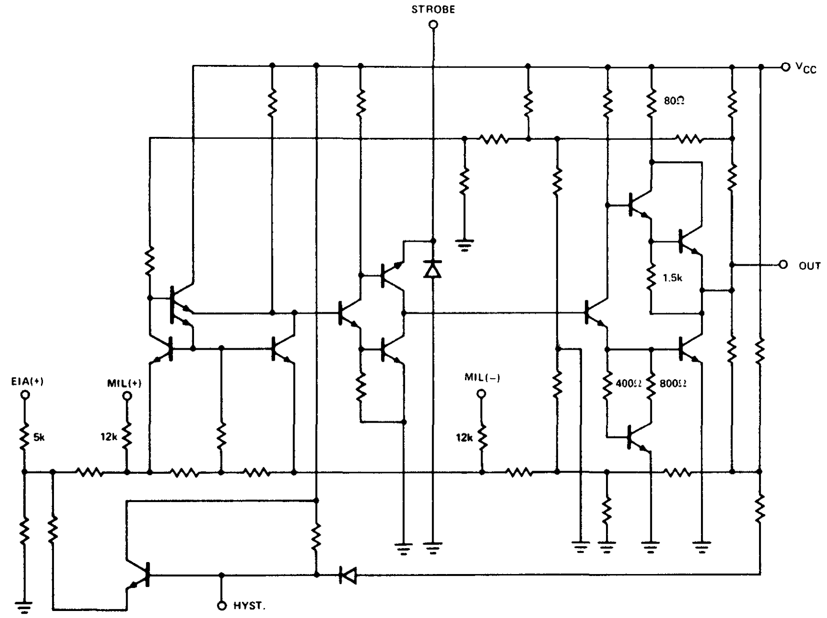
T_A = 25° C and V_{CC} = 5.0V (Cont'd)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
					INPUTS					OUTPUTS	
	MIN.	TYP.	MAX.	UNITS	EIA	MIL(+)	MIL(-)	HYS	STROBE		
"1" Output Voltage (EIA) ("Hysteresis" open)	2.8	3.5		V	+1.2V	0V	0V		2.0V	-800μA	8, 12
"1" Output Voltage (MIL)	2.8	3.5		V		+0.35V	0V		2.0V	-800μA	8, 13
"0" Output Voltage (EIA) ("Hysteresis" open)		0.2	0.4	V	-1.2V	0V	0V		2.0V	9.6mA	9, 10
"0" Output Voltage (MIL)		0.2	0.4	V		-0.35V	0V		2.0V	9.6mA	9, 11
Input Resistance (EIA)	3	5	7	kΩ	±25V	0.0V	0.0V				
Input Resistance (MIL)	7.5	11.4		kΩ	0.0V	±25V	0.0V				
Power Consumption (per receiver)		44	75	mW	3.0V	0V	0V				17
Output Short Circuit Current	-10		-70	mA	-3.0V	0.0V	0.0V		5.00V	0.0V	16, 17
Propagation Delay		100	150	ns					5.00V		14
Signal Switching Acceptance	20			kHz					5.00V		

NOTES:

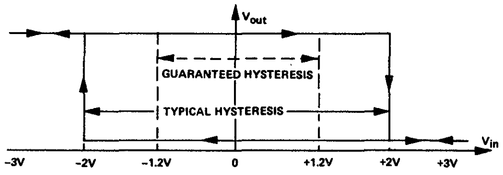
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. This test guarantees operation free of latch-up over the specified input voltage range.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Previous EIA input: +3V (See hysteresis curve).
11. Previous MIL input: +0.9V (See hysteresis curve).
12. Previous EIA input: -3V (See hysteresis curve).
13. Previous MIL input: -0.9V (See hysteresis curve).
14. Reference AC Test Figure.
15. This test guarantees transfer of signals of up to 20kHz. Connect 1000pF between the output terminal and ground.
16. Each receiver to be tested separately.
17. V_{CC} = 5.25V.

SCHEMATIC DIAGRAM

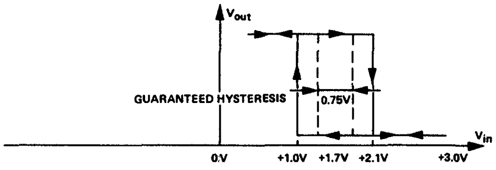


HYSTERESIS CURVES

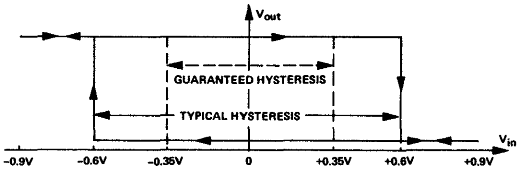
EIA – "HYSTERESIS" OPEN



EIA – "HYSTERESIS" GROUNDED

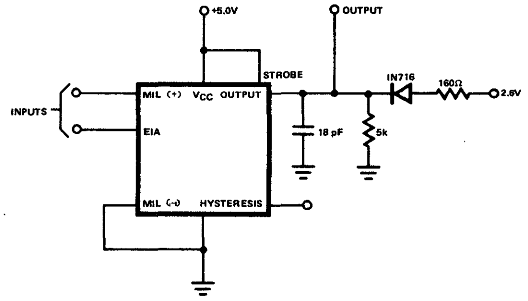


MIL – HYSTERESIS

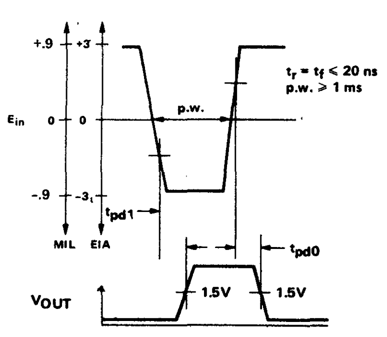


*V_{in} IS REFERENCED TO THE MIL (–) INPUT TERMINAL

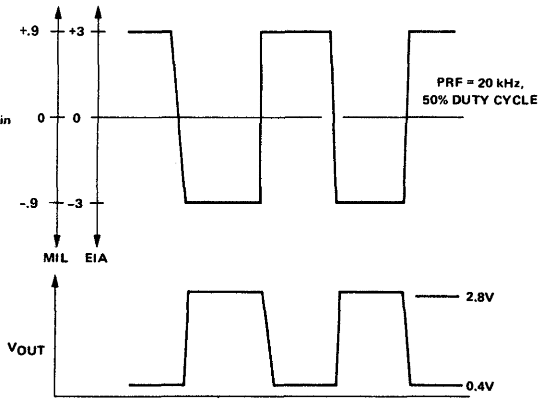
AC TEST FIGURE AND WAVEFORMS



PROPAGATION DELAY

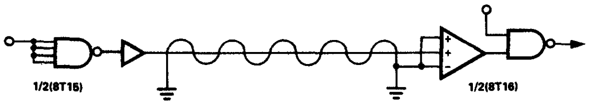


SIGNAL SWITCHING ACCEPTANCE

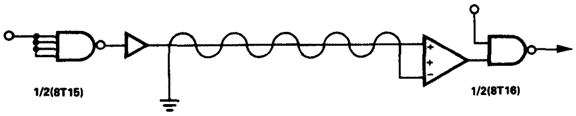


TYPICAL APPLICATIONS

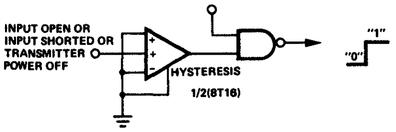
HIGH DIFFERENTIAL NOISE IMMUNITY
(EIA + INPUT)



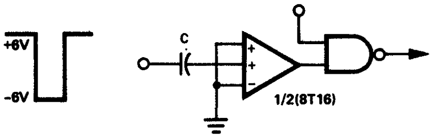
HIGH COMMON MODE NOISE IMMUNITY
(MIL + INPUT)



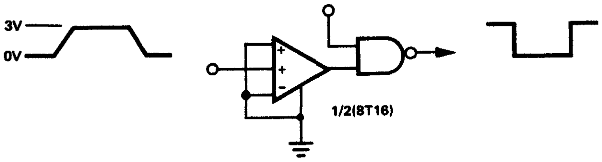
EIA FAIL-SAFE OPERATION



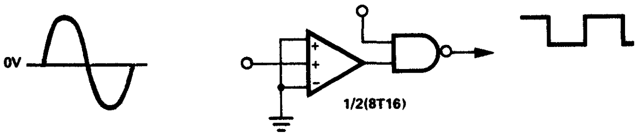
AC COUPLED OPERATIONS



SCHMITT TRIGGER



SINE TO SQUARE WAVE CONVERTER



BIDIRECTIONAL ONE SHOT

8T20

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The Bidirectional One Shot is intended for applications where high speed low level signal processing is required.

The 8T20 is a Monolithic Building Block, consisting of a high speed analog comparator, digital control circuitry, and a precision monostable multivibrator. The differential input threshold voltage is between ±4mV with respect to the input reference level which may range from -3.2V to +4.2V. For input frequencies up to 8MHz, the device may be conditioned to act as a frequency doubler since it can trigger on both positive and negative input transitions.

Timing pins permit using this device in a variety of applications where external control over pulse width is desirable. Pulse width (t_W) is defined by the relationship $t_W = C_X R_X \text{Log}_e 2$. Pulse width stability is internally compensated and virtually independent of temperature and V_{CC} variations, thus only limited by the accuracy of external timing components.

An internal resistive divider is available on the chip to provide a voltage of 1.4V (typ.). This output can be connected directly to either of the comparator inputs as a reference voltage when interfacing with TTL outputs.

ABSOLUTE MAX RATINGS

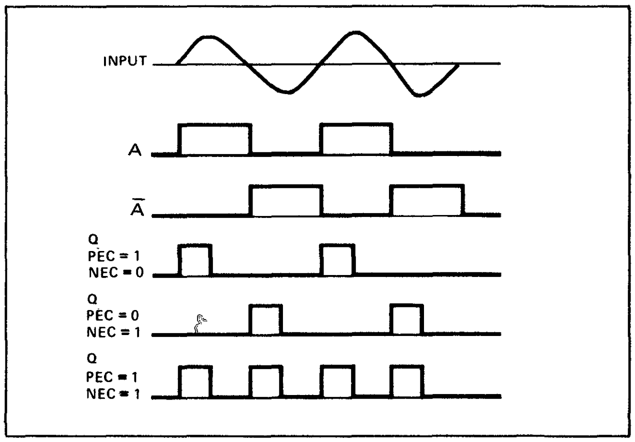
Input Voltage

V_{CC}:	+7
V_{EE}:	-7

APPLICATIONS

DISC, TAPE AND DRUM READERS
DIGITAL COMMUNICATIONS RECEIVERS
SIGNAL CONDITIONERS
TRANSITION DETECTORS

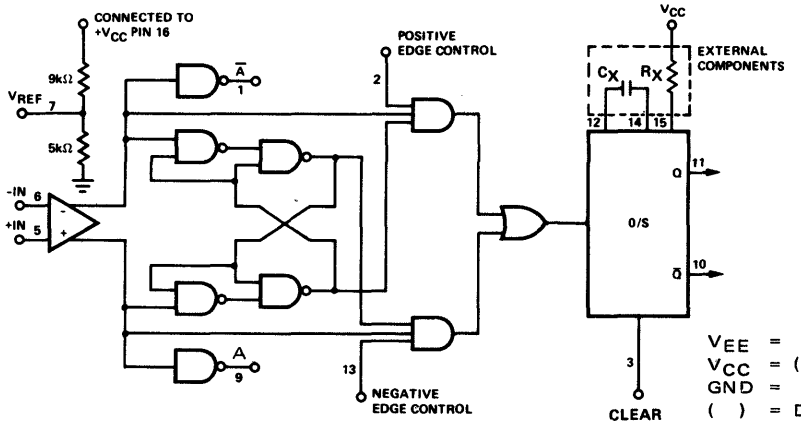
INPUT/OUTPUT WAVEFORMS



FEATURES

- DIFFERENTIAL INPUT THRESHOLD = ±4mV
- PULSE POSITION ERROR = TYPICALLY <3ns
- MAX. INPUT FREQUENCY = 8 MHz
- TRIGGERS ON POSITIVE AND/OR NEGATIVE TRANSITIONS

LOGIC DIAGRAM



V_{EE} = (4) (-5V ±5%)
V_{CC} = (16) (+5V ±5%)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Temperature Range and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"1" Output Voltage (All Outputs)	2.6			V	I_{out} = -800uA	7
"0" Output Voltage (All Outputs)			0.4	V	I_{out} = +16mA	8
DIFFERENTIAL INPUTS						
Input Threshold Voltage (V_T)			±4	mV		10
Input Bias Current			125	uA	Figure 5	
Input Offset Current		2		uA		
Common Mode Input Volt, Range	-3.2		+4.2	V		12
DIGITAL INPUTS						
"1" Input Current			40	uA	V_{in} = 4.5V	
"0" Input Current						
PEC. NEC			-2.4	mA	V_{in} = 0.4V	
Clear			-1.6	mA	V_{in} = 0.4V	
Input Latch Voltage	5.5			V	I_{in} = 10mA	9
Reference Voltage (V_{REF})	0.8	1.4	2.0	V	Pin 7 tied to Pin 6	
Output Pulse Width, Fig. 1	10		40	ns	Rx = 10K, Cx = Open	11
Output Pulse Width, Fig. 3	600		800	ns	Rx = 10K, Cx = 100pf	11
Power Supply Current						
I_{CC}			55	mA	Vcc = +5.25V	
I_{EE}			-20	mA	Vcc = -5.25V	
Short Circuit Current (I_{SO})	-20		-70	mA		

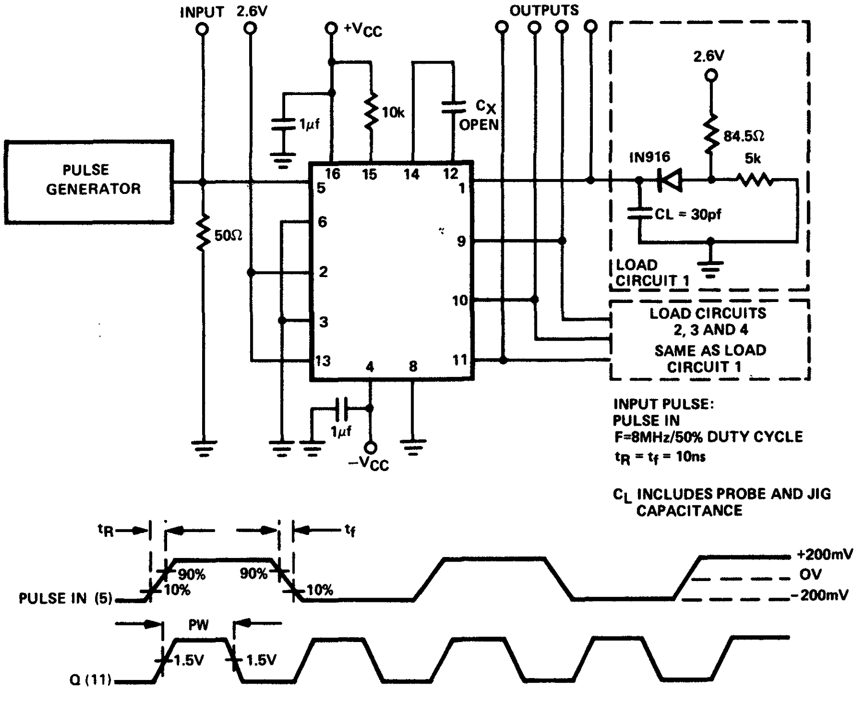
$T_A = 25°C, V_{CC} = +5.00V, V_{EE} = -5.00V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Output Frequency	16			MHz	Fig. 1, f_{in} = 8 MHz	11
Propagation Delay (ton, toff)						
Input to Q, $\overline{Q}$		30	50	ns	Fig. 2	11
Input to A, $\overline{A}$		30	50	ns	Fig. 4	11
Clear to Q, $\overline{Q}$		20	30	ns		

NOTE:

1. All Voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward based.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is applied through a resistor to ground.
8. Output sink current is supplied through a resistor to Vcc.
9. This test guarantees operation free of Input latch up over the specified operating supply voltage range.
10. The differential input threshold voltage (V_T) is defined as the maximum DC voltage deviation from the reference level necessary to trigger the one-shot.
11. *Refer to AC test circuits.*
12. Common mode voltages that are confined within the dynamic range as specified will not cause false triggering of the one-shot.

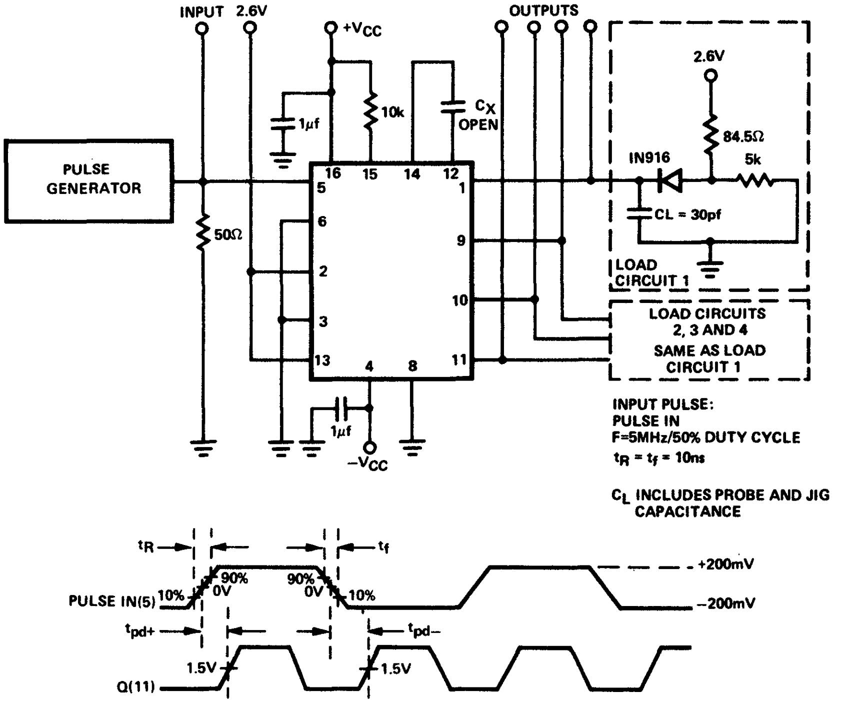
AC TEST CIRCUITS



INPUT PULSE:
PULSE IN
F=8MHz/50% DUTY CYCLE
$t_R = t_f = 10ns$

C_L INCLUDES PROBE AND JIG CAPACITANCE

FIGURE 1

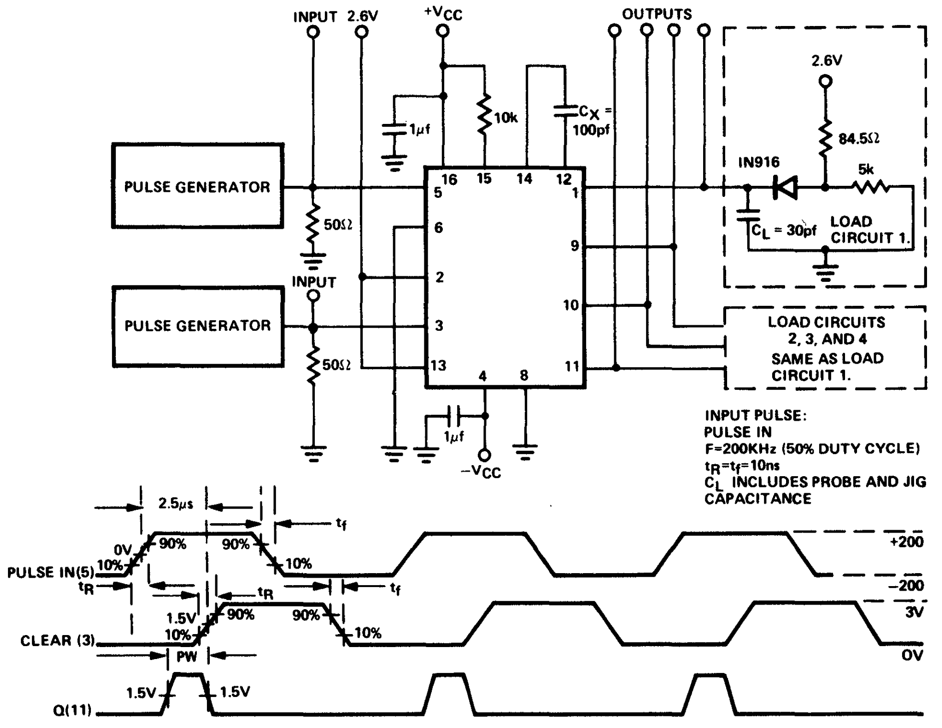


INPUT PULSE:
PULSE IN
F=5MHz/50% DUTY CYCLE
$t_R = t_f = 10ns$

C_L INCLUDES PROBE AND JIG CAPACITANCE

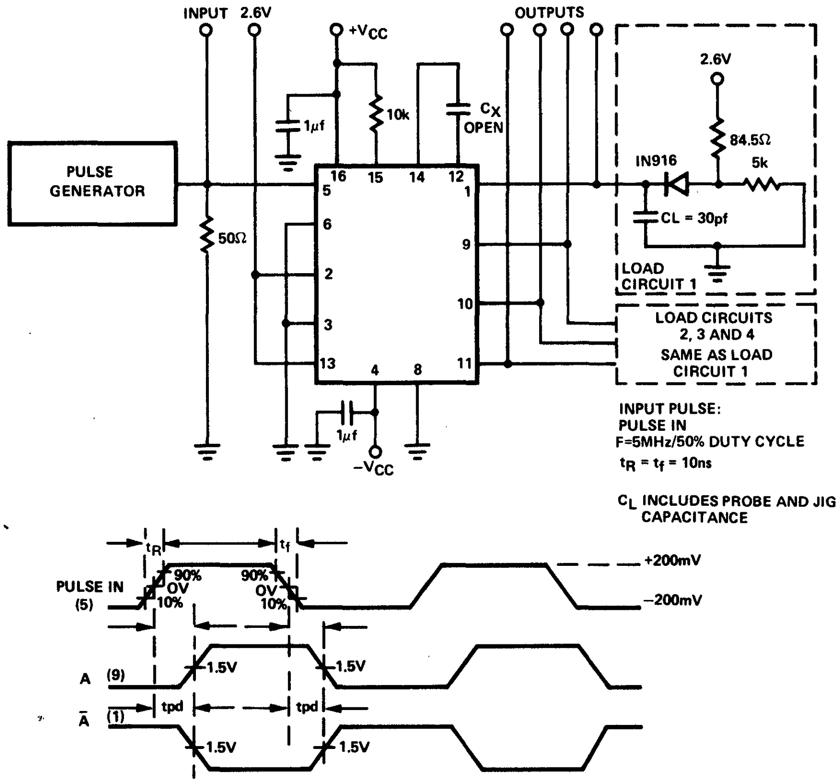
FIGURE 2

AC TEST CIRCUITS (Cont'd)



INPUT PULSE:
PULSE IN
F=200KHz (50% DUTY CYCLE)
$t_R = t_f = 10ns$
C_L INCLUDES PROBE AND JIG CAPACITANCE

FIGURE 3



INPUT PULSE:
PULSE IN
F=5MHz/50% DUTY CYCLE
$t_R = t_f = 10ns$

C_L INCLUDES PROBE AND JIG CAPACITANCE

FIGURE 4

INPUT BIAS CURRENT TEST CIRCUIT

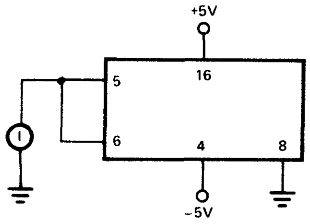


FIGURE 5

RETRIGGERABLE ONE-SHOT

8T22

PRODUCT AVAILABLE IN 0°C TO +75°C TEMP. RANGE ONLY.

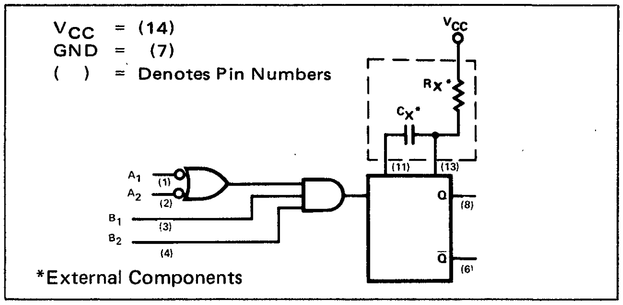
DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The Signetics N8T22A is a direct pin-for-pin replacement for the 9601 retriggerable one-shot. Triggering can be performed on either the leading or falling edge of the input signal through selection of the proper input terminal.

The inputs are level-sensitive making triggering independent of signal transition times. Output pulse width is determined by external timing components (R_X and C_X) with each trigger pulse initiating a complete new timing cycle.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
"1" Output Voltage	2.4	3.4		V	I_{out} = −960μA
"0" Output Voltage		0.2	0.45	V	I_{out} = 12.8mA
Input HIGH Voltage	1.9			V	
Input LOW Voltage			0.9	V	
"0" Input Current			1.6	mA	V_{in} = 0.45V
"1" Input Current			60	μA	V_{in} = 4.5V
Timing Resistor	5.0		50	kΩ	
C_{Stray} - Maximum allowable wiring capacitance			50	pF	P13 to Ground

T_A = 25° C and V_{CC} = 5.0V

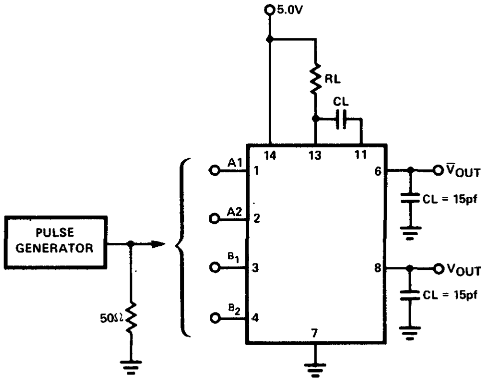
CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Propagation Delay					
Negative Trigger Input to True Output (t_{pd}+)		25	40	ns	R_x = 5.0kΩ, C_x = 0 C_L = 15pf
Negative Trigger Input to False Output (t_{pd}-)		25	40	ns	R_x = 5.0kΩ, C_x = 0 C_L = 15pF
Min. True Output Pulse Width		45	65	ns	R_x = 5.0kΩ, C_x = 0 C_L = 15pF
Pulse Width Variation	3.08	3.42	3.76	μs	R_x = 10kΩ, C_x = 1000pF
Short Circuit Current	-10		-40	mA	V_{out} = 0V
Power Supply Current			25	mA	V_{CC} = 5.25V

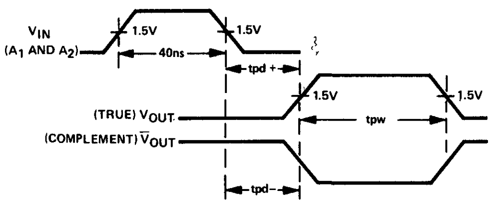
NOTES:

1. Positive current is defined as into the pin referenced.
2. Unless otherwise noted, 10kΩ resistor placed between Pin 13 and V_{CC} (R_x).
3. Manufacturer reserves the right to make design and process changes and improvements.

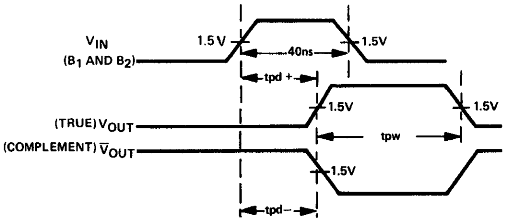
AC TEST FIGURE AND WAVEFORMS

TRIGGER INPUT/OUTPUT AND PULSE WIDTH





WAVEFORM A.



WAVEFORM B.

NOTES:

1. Pulse Generator has the following characteristics: $t_r = t_f$ = 10ns (10% to 90%), AMP. = 3V.
2. C_L includes probe and jig capacitance.
3. For tpd+, tpd- and tpw (min.) RX = 5kΩ ± 1%, CX = OPEN, PRR = 1MHz.
4. For Δtpw: RX = 10kΩ ± 1%, C_X = 1000pF ± 1%, PRR = 200kHz.

DUAL LINE DRIVER | 8T23

0°C to +75°C

DIGITAL 8000 SERIES TTL MSI

DESCRIPTION

The 8T23 is a Dual Line Driver designed to meet all of the requirements of the IBM System/360 I/O Interface Specification for interface drivers.

The low impedance emitter follower output will drive terminated lines such as coaxial cable or twisted pair. The output is protected against accidental shorting by an internal clamping network which turns on once the output voltage drops below approximately 1.5 volts. The uncommited emitter output structure allows Dot-OR logic to be performed as in "Party-Line" operations.

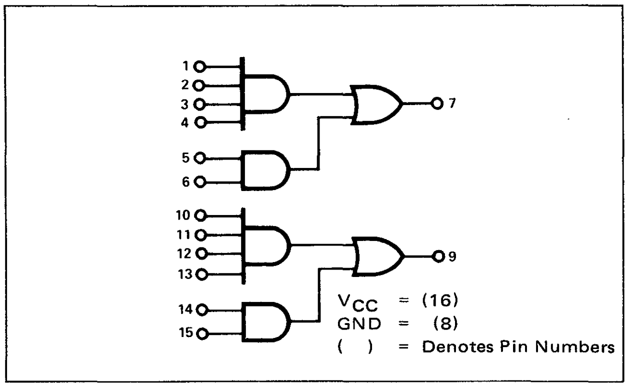
Multiple emitter inputs allow the 8T23 to interface with standard TTL or DTL systems and the circuit operates from a single +5 volt power supply.

Additional logic incorporated in the 8T23 Dual Line Driver can be used during the power-up and power-down sequence to ensure that no spurious noise is generated on the line.

FEATURES

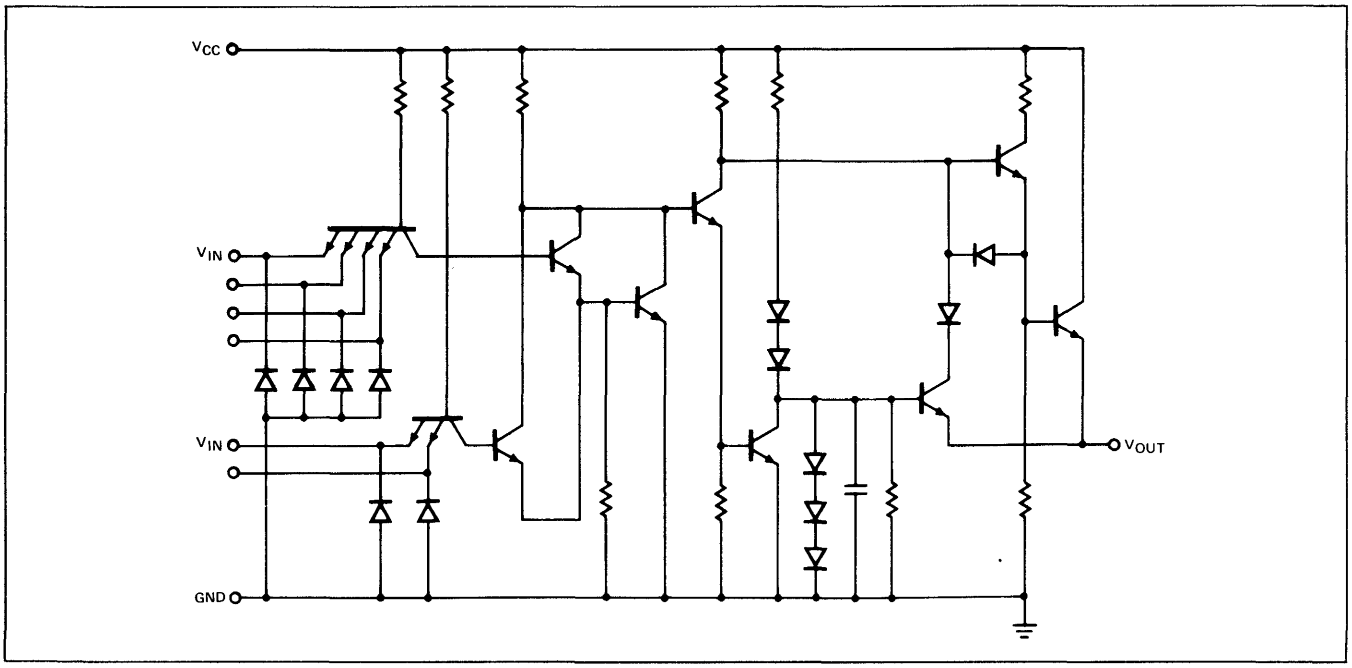
- I_{OUT} = 59.3mA AT 3.11 VOLTS
- UNCOMMITTED EMITTER OUTPUT STRUCTURE FOR PARTY-LINE OPERATION
- SHORT-CIRCUIT PROTECTION
- SINGLE 5 VOLT POWER SUPPLY
- AND-OR LOGIC CONFIGURATION

LOGIC DIAGRAM WITH PIN LAYOUT



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0°C TO +75°C)

CHARACTERISITCS	LIMITS				TEST CONDITIONS				NOTES
	MIN	TYP	MAX	UNITS	AND GATE #1		INPUTS OF #2 AND GATE	OUTPUT	
					INPUT UNDER TEST	OTHER INPUT			
"0" Output Voltage			+0.15	V	0.8V	4.5V	OV	-240μA	7
"1" Output Leakage Current			40	μA	OV	OV	OV	3.0V	1, 15
"0" Input Current	-0.1		-1.6	mA	0.4V	4.5V			
"1" Input Current			40	μA	4.5V	OV			

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

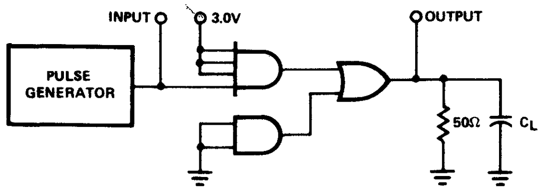
CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
	MIN	TYP	MAX	UNITS	AND GATE #1		INPUTS OF #2 AND GATE	OUTPUT	
					INPUT UNDER TEST	OTHER INPUT			
"1" Output Voltage	3.11			V	2.0V	2.0V	0.8V	59.3mA	
Turn-on Delay		12 15	20 25	nS nS					8, 13 9, 13
Turn-off Delay		12 20	20 35	nS nS					8, 13 9, 13
Power/Current Consumption									
Output at "0"			315/ 60	mW/ mA	0.8V	0.8V	0.8V		12, 16
Output at "1"			150/ 28	mW/ mA	2.0V	2.0V	2.0V		12, 16
Input Latch Voltage	5.5			V	10mA	OV	OV		11
"1" Output Current	-100		-250	mA	4.5V	4.5V	OV	2.0V	14
Input Clamp Voltage			-1.5	V	-12mA				14

NOTES:

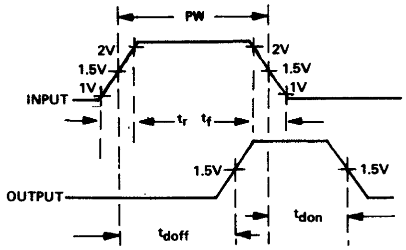
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. With forced output current of 240μA the output voltage must not exceed 0.15V.
8. RL = 50Ω to ground.
9. Load is 50Ω in parallel with 100pF.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
12. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition for both drivers.
13. Reference AC Test Circuit and Pulse Requirements.
14. Reference "Typical Output Current vs. Output Voltage Curve".
15. V_{CC} = 0.00V.
16. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS

AC TEST CIRCUIT



PULSE REQUIREMENTS



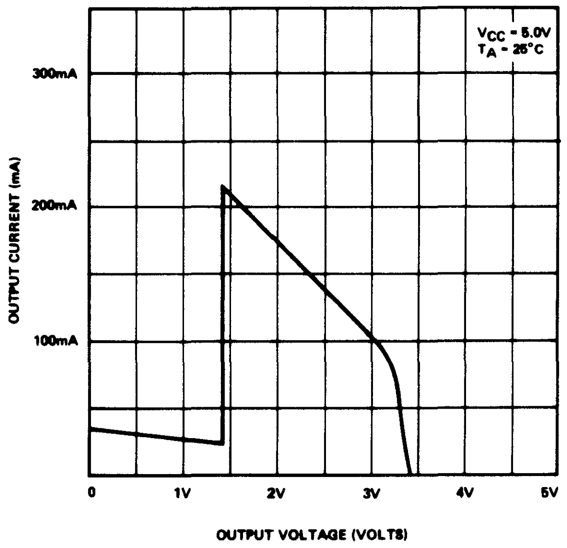
INPUT PULSE:

AMPLITUDE = 3.0V

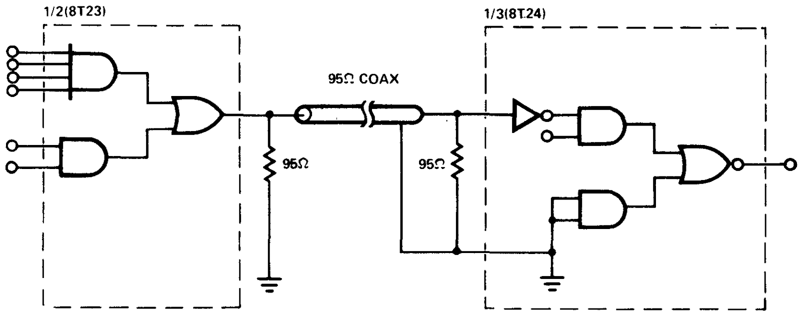
PW. = 50ns (50% DUTY CYCLE)

$t_r = t_f \leqslant 5ns$ (10% AND 90% MEASUREMENT POINTS)

TYPICAL OUTPUT CHARACTERISTICS



TYPICAL APPLICATIONS



TRIPLE LINE RECIEVER | 8T24

0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System/360 I/O Interface Specification (File No. S360-19). Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of 0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The 8T24 will also withstand an input of -0.15V with power on or off.

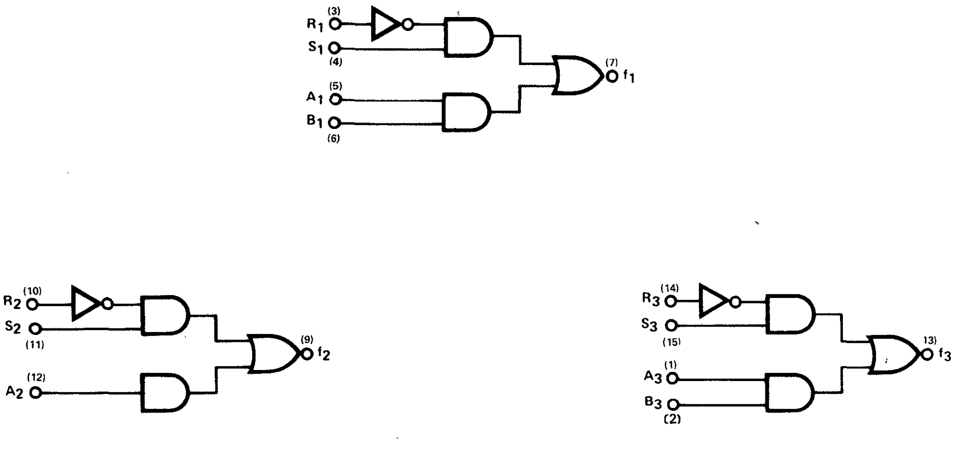
The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

FEATURES

- BUILT–IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $T_{ON} = T_{OFF} = 20$ns (TYPICAL)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5V POWER SUPPLY

* Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

LOGIC DIAGRAM WITH PIN LAYOUT



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±5%, T_A = 0°C TO +75°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
"1" Output Voltage	2.6	3.4		V	1.70V	4.5V	OV	OV	-800μA	7
	2.6	3.4		V	OV	0.7V	OV	OV	-800μA	7
"0" Output Voltage		0.2	0.4	V	0.70V	1.7V	OV	OV	16mA	8
		0.2	0.4	V	OV	OV	1.7V	1.7V	16mA	8
"0" Input Current										
S_n	-0.1		-1.6	mA	OV	0.4V				
A_n	-0.1		-1.6	mA	OV		0.4V			
B_n	-0.1		-1.6	mA				0.4V		
"1" Input Current										
R_n			0.17	mA	3.11V					
R_n			5.0	mA	7.0V					
R_n			5.0	mA	6.0V					9
S_n			40	μA	3.11V	4.5V				
A_n			40	μA			4.5V	OV		
B_n			40	μA			OV	4.5V		

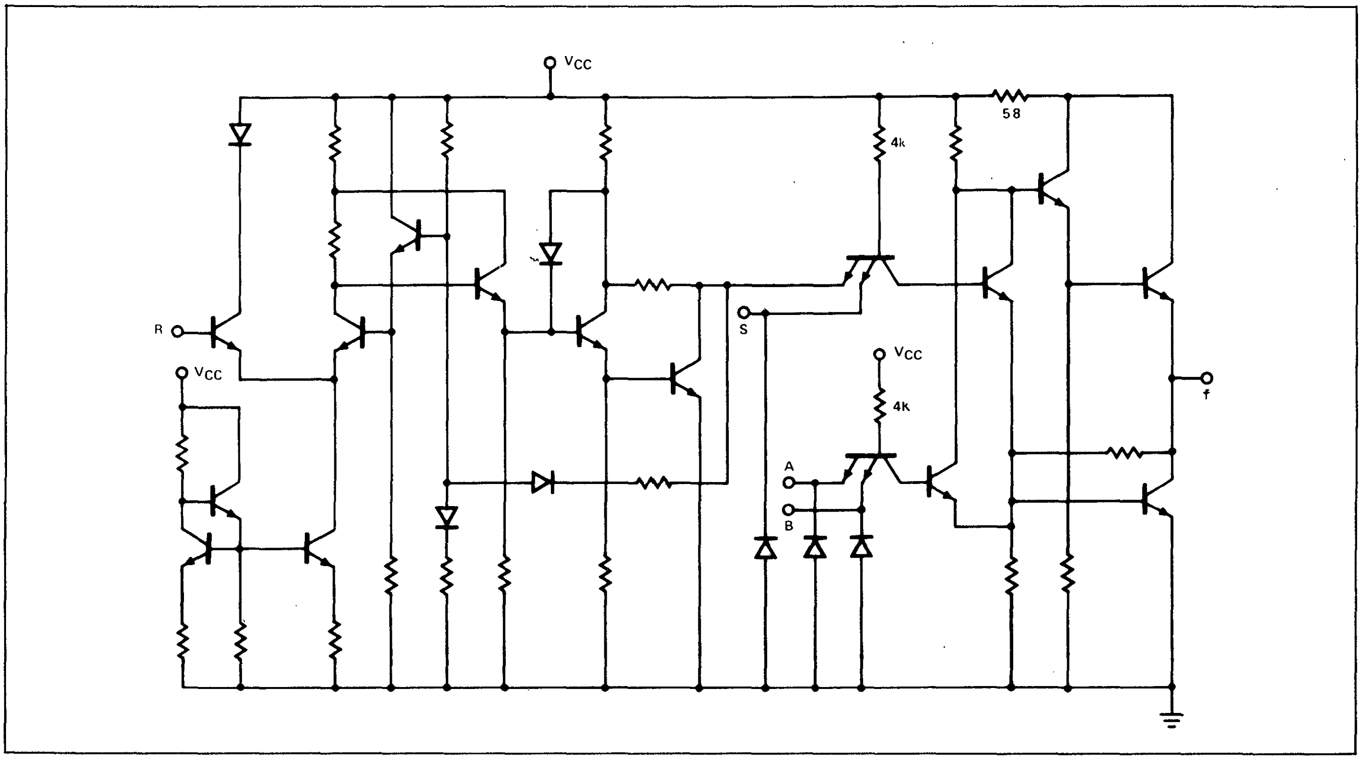
ELECTRICAL CHARACTERISTICS (AT V_{CC}= 5.0v AND T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
Turn-on Propagation Delay		20	30	nS						13
Turn-off Propagation Delay		20	30	nS						13
Hysteresis	0.2	0.4		V		4.5V	0V	0V		11, 12
Power/Current Consumption		315 60	380 72	mW mA						14
Input Latch Voltage:										
S	5.5			V	3.11V	10mA	0V	0V		10
A	5.5			V	0V	0V	10mA	0V		10
B	5.5			V	0V	0V	0V	10mA		10
Output Short Circuit Current	-50		-100	mA	3.11V	0V	0V	0V		
Input Clamp Voltage										
S			-1.5	V		-12mA				
A			-1.5	V			-12mA			
B			-1.5	V				-12mA		

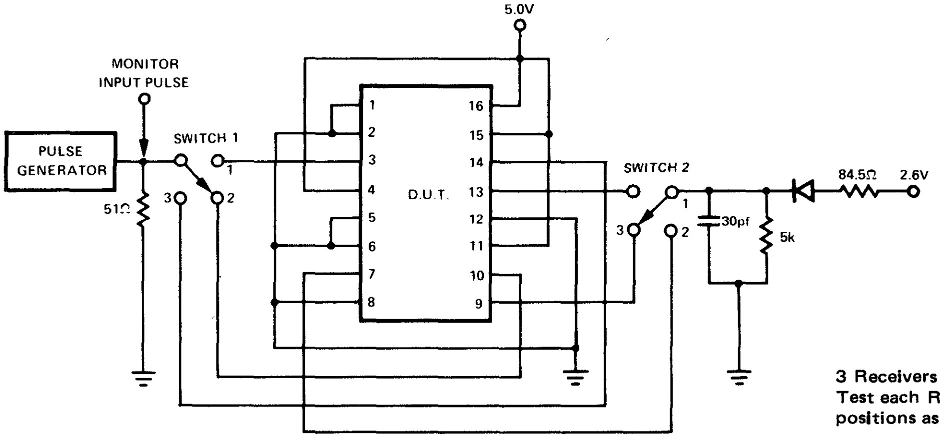
NOTES:

1. All voltage measurments are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is applied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. V_{CC} = 0.00V
10. This test guarantees operation free of Input latch up over the specified operating supply voltage range.
11. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "O" to "1" state and the level at which the output begins to go from "1" to "0".
12. See Hysteresis test circuit.
13. Refer to AC test circuits.
14. V_{CC} = 5.25V.

CIRCUIT SCHEMATIC



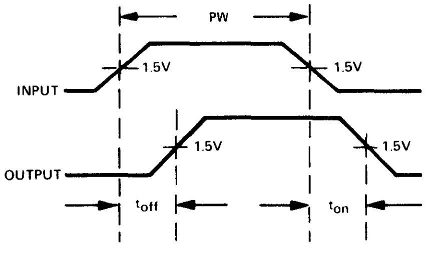
AC TEST CIRCUIT AND WAVEFORMS



3 Receivers in the package. Test each Receiver using switch positions as shown in Table I.

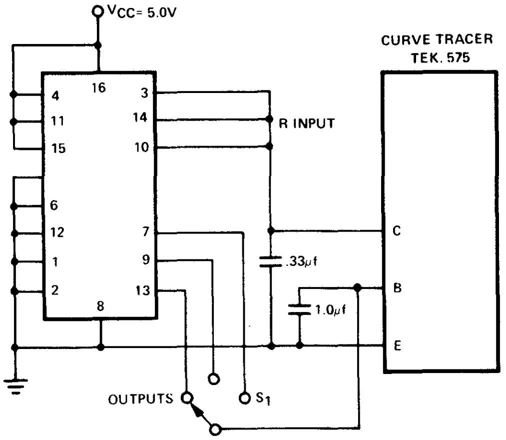
TABLE I

Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3



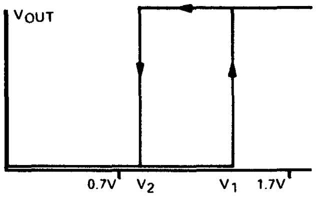
Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

HYSTERESIS TEST CIRCUIT

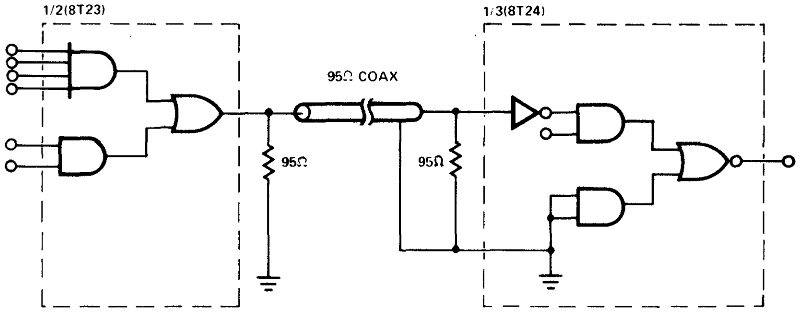


Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.7V minimum and 1.7 maximum.
2. Hysteresis = $V_1 - V_2$



TYPICAL APPLICATION



QUAD BUS DRIVER/RECEIVER

8T26

0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T26 bus driver/receiver contains four pair of inverting logic gates along with two buffered common enable lines.

Both the driver and receiver gates have tri-state outputs and PNP inputs. Tri-state outputs provide the high switching speeds of totem pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200 μA maximum.

A logic "1" on the bus enable (B/E) input allows input data to be transferred to the output of the driver, while a logic "0" will force the output to a high impedance state and will also disable the PNP resulting in negligible input load current. The driver gate will sink 50mA of current with a maximum V_{CE} of 0.45V.

The receiver gate is enabled by a logic "0" on the input enable (I/E) pin and provides 16mA current sink capability;

FEATURES

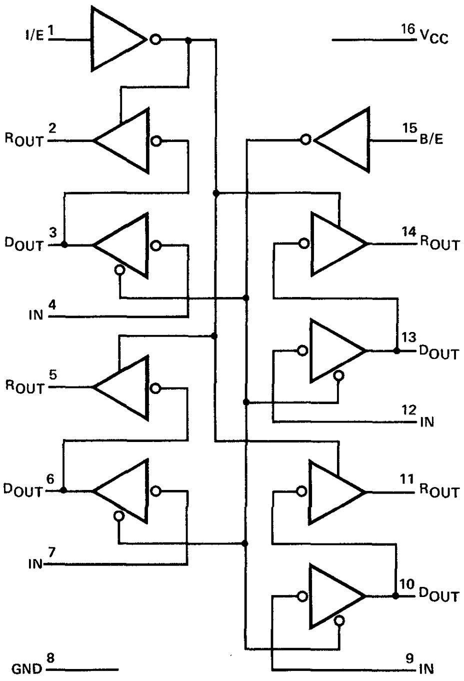
- SCHOTTKY-CLAMPED TTL
- PROPAGATION DELAY = 17nS (MAX.)
- TRI-STATE OUTPUTS
- PNP INPUTS
- 40mA CURRENT SINK CAPABILITY
- SBD* INPUT CLAMPS

*SCHOTTKY-BARRIER-DIODE

APPLICATIONS

- HALF-DUPLEX DATA TRANSMISSION
- ROUTING DATA IN BUS-ORIENTED SYSTEMS
- HIGH CURRENT DRIVERS

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_A = 0°C to 75°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION
$I(0)_{in}$	Input "0" current (All Inputs)			–200	µA	V_{in} = 0.4
$I(1)_{in}$	Input "1" current Pins 1, 4, 7, 9, 12, 15			25	µA	V_{in} = 5.25
$V(0)_{in}$	Input (0) Threshold voltage	0.85			Volts	
$V(1)_{in}$	Input (1) Threshold voltage			2	Volts	
$V(1)_{out}$	Output (1) voltage Pins 3, 6, 10, 13	2.6	3.3		Volts	I_{out} = –10.0mA
$V(1)_{out}$	Output (1) voltage Pins 2, 5, 11, 14	2.6	3.3		Volts	I_{out} = –2.0mA
$V(0)_{out}$	Output (0) voltage Pins 3, 6, 10, 13		0.2	0.45	Volts	I_{out} = 50mA
$V(0)_{out}$	Output (0) voltage Pins 2, 5, 11, 14		0.2	0.45	Volts	I_{out} = 16mA
$I(1)_{off}$	Output (1) off/Leakage current			100	µA	V_{out} = 2.6V
$I(0)_{off}$	Output (0) off/Leakage current			–100	µA	V_{out} = 0.45V
V_{cin}	Input/Clamp/Voltage			–1.0	Volts	I_{in} = –5mA
I_{so}	Output (1) short circuit current - - Pins 3, 6, 10, 13	–50		–150	mA	V_o = 0 Volts*
I_{so}	Output (1) short circuit current - - Pins 2, 5, 11, 14	–30		–75	mA	V_o = 0 Volts*
I_{CC}	Power supply current			80	mA	V_{CC} = 5V

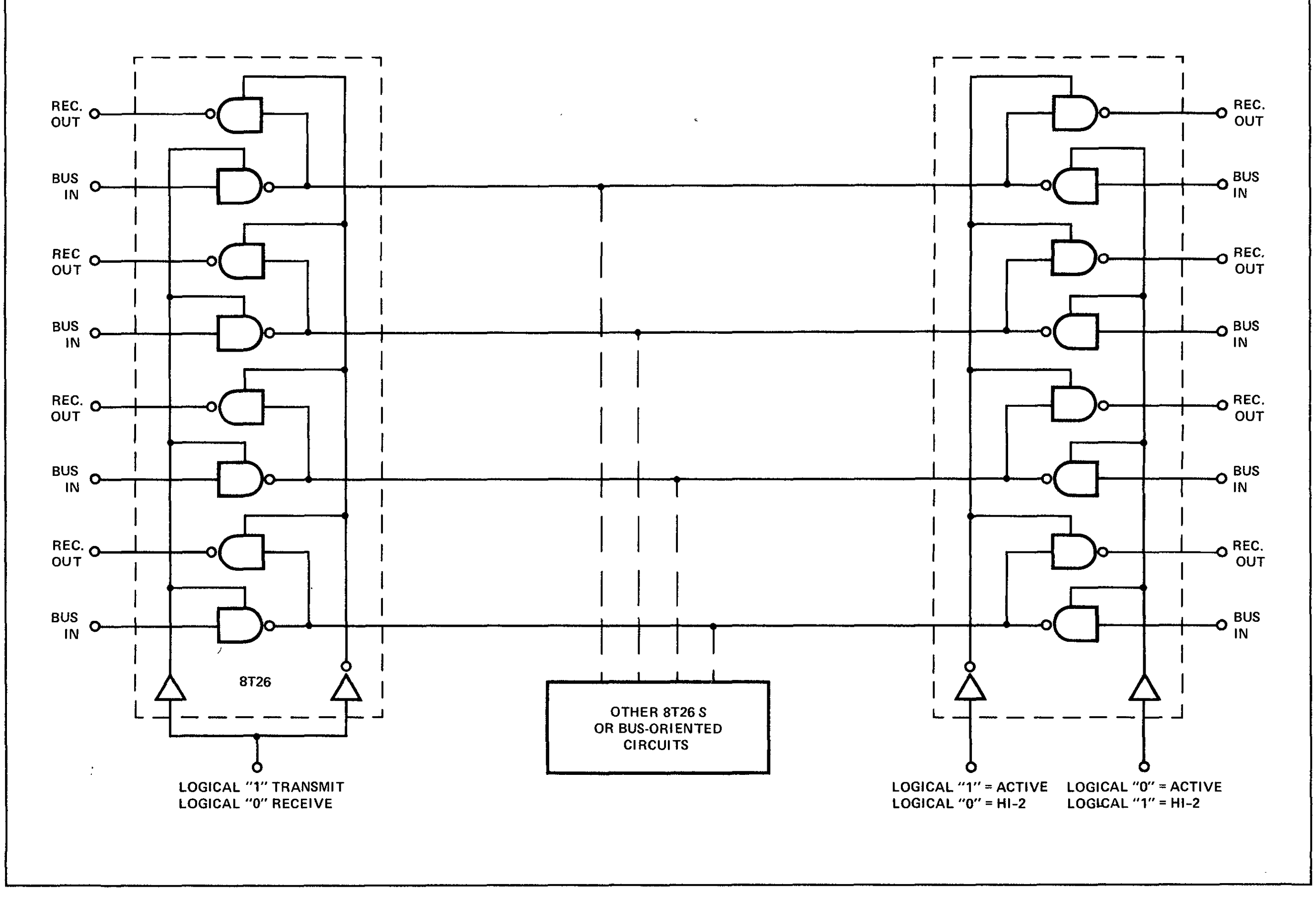
T_A = 25°C, V_{CC} = 5.00V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION
T_{on}	Turn on delay Pins 2, 5, 11, 14			10	nsec	30 pF, 300 ohm
T_{off}	Turn off delay Pins 2, 5, 11, 14			15	nsec	30 pF, 300 ohm
T_{on}	Turn on delay Pins 3, 6, 10, 13			17	nsec	150 pF, 100 ohm
T_{off}	Turn off delay Pins 3, 6, 10, 13			17	nsec	150 pF, 100 ohm

*Do not ground more than one output at a time.

TYPICAL APPLICATION

BI DIRECTIONAL DATA BUS



SECTION 7
SCHOTTKY 82S MSI

DESCRIPTION

Series 82S Schottky TTL circuits are implemented with Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

The Schottky-clamped transistors are formed by using Schottky-barrier-diodes in parallel with the base-collector junctions. This is realized physically by depositing metal over the base and N region of the collector forming a metal-silicon diode. The effect of this diode, which has a lower forward voltage than the collector-base function is to hold the transistor out of saturation by diverting most of the excess base current. The reduction in stored-charge plus the use of smaller geometries results in a major improvement of switching characteristics.

By eliminating gold-doping normally employed in conventional TTL processing to reduce storage time, PNP transistors can be used to advantage by the circuit designers.

In 82S MSI, PNP transistors are used to reduce input loading as illustrated in Fig. 1. Maximum low level input current is specified at 400 μA which allows the systems designer to upgrade existing designs without encountering fanout limitations.

FEATURES

- 3ns TYPICAL GATE PROPAGATION DELAY
- 20mW PER-GATE TYPICAL POWER DISSIPATION
- LOW LEVEL INPUT CURRENT (PER UNIT LOAD = .4mA (MAX.)

EASE OF SYSTEM DESIGN

- FULLY COMPATIBLE WITH SERIES 8000, 54/74 TTL, AND MOST DTL
- SCHOTTKY-DIODE-CLAMPED INPUTS SIMPLIFY SYSTEM DESIGN
- TERMINATED, CONTROLLED-IMPEDANCE LINES NOT NORMALLY REQUIRED
- LOW OUTPUT IMPEDANCE: PROVIDES LOW AC NOISE SUSCEPTABILITY AND DRIVES HIGHLY CAPACITIVE LOADS

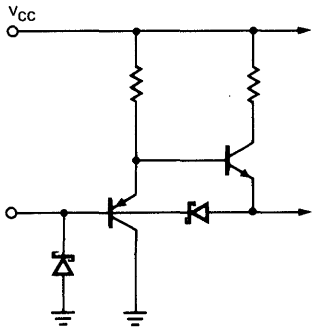


Figure 1

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted)

SUPPLY VOLTAGE V_{CC}	+7V
INPUT VOLTAGE	+6V
OUTPUT VOLTAGE	+7V
OPERATING FREE-AIR TEMPERATURE RANGE	0°C to 75°C

8-INPUT DIGITAL MULTIPLEXER

82S30

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 82S30 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, the f output is unconditionally low and the $\bar{f}$ output is unconditionally high.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- DIRECT OUTPUT INHIBIT
- 82S30 CAN REPLACE 9312 FOR HIGHER SPEED

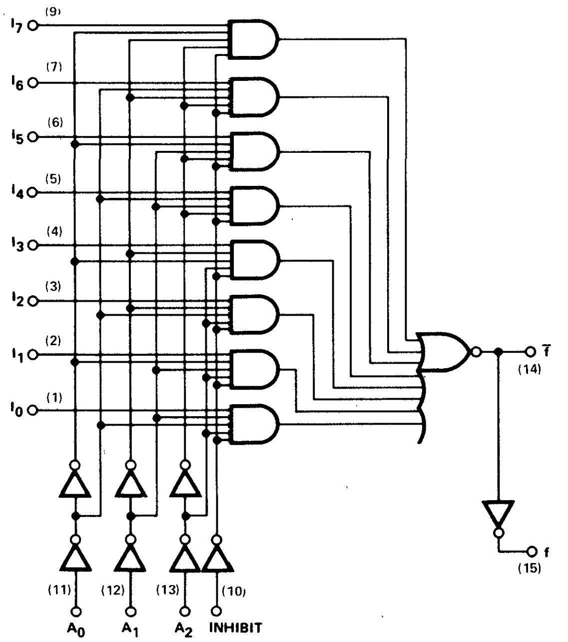
TRUTH TABLE

ADDRESS			DATA INPUT									OUTPUT	
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	f	82S30 $\bar{f}$
0	0	0	x	x	x	x	x	x	x	1	0	1	0
0	0	1	x	x	x	x	x	x	1	x	0	1	0
0	1	0	x	x	x	x	x	1	x	x	0	1	0
0	1	1	x	x	x	x	1	x	x	x	0	1	0
1	0	0	x	x	x	1	x	x	x	x	0	1	0
1	0	1	x	x	1	x	x	x	x	x	0	1	0
1	1	0	x	1	x	x	x	x	x	x	0	1	0
1	1	1	1	x	x	x	x	x	x	x	0	1	0
0	0	0	x	x	x	x	x	x	x	0	0	0	1
0	0	1	x	x	x	x	x	x	0	x	0	0	1
0	1	0	x	x	x	x	x	0	x	x	0	0	1
0	1	1	x	x	x	x	0	x	x	x	0	0	1
1	0	0	x	x	x	0	x	x	x	x	0	0	1
1	0	1	x	x	0	x	x	x	x	x	0	0	1
1	1	0	x	0	x	x	x	x	x	x	0	0	1
1	1	1	0	x	x	x	x	x	x	x	0	0	1
x	x	x	x	x	x	x	x	x	x	x	1	0	1

x = don't care

LOGIC DIAGRAM

82S30



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	A_1	A_2	A_3	INH	DATA INPUT I_n	OUTPUTS	
"1" Output Voltage, Output f	2.7			V	*	*	*	0.8V	2.0V	−1.0mA	6,11
Output $\overline{f}$	2.7			V	*	*	*	2.0V	*	−1.0mA	6,11
"0" Output Voltage			0.5	V	0.8V	0.8V	0.8V	0.8V	0.8V	20mA	7,14
"1" Input Current											
Inputs A_n, I_n			10	μA	4.5V	4.5V	4.5V		4.5V		
Input INH			10	μA				4.5V			
"0" Input Current											
A_n, I_n, INH			−400	μA	0.5V	0.5V	0.5V		0.5V		

T_A = 25°C and V_{CC} = 5.0V

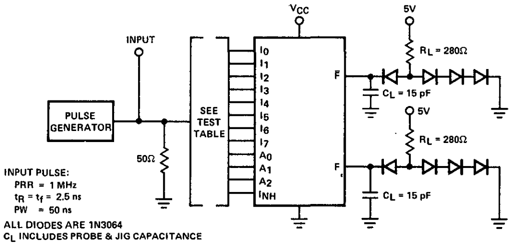
CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
									DATA INPUT	OUTPUTS		
	MIN	TYP	MAX	UNITS	A	A	A	INH	I_n	f	$\overline{f}$	
Propagation Delay			20	ns								
A_n to f												
A_n to $\overline{f}$			17	ns								8
I_n to $\overline{f}$			12	ns								8
INH to $\overline{f}$			16	ns								8
Power Consumption/Supply Current			62	mA	4.5V	4.5V	4.5V	4.5V	0V			11
Output Short Circuit Current												
Output f	−40		−100	mA	0V	0V	0V	0V	4.5V	0V		
Output $\overline{f}$	−40		−100	mA	0V	0V	0V	0V	0V		0V	
Input Clamp Voltage	−1.2			V	−18 mA	−18 mA	−18 mA	−18 mA				12

*See Truth Table for Logical Conditions

NOTES:

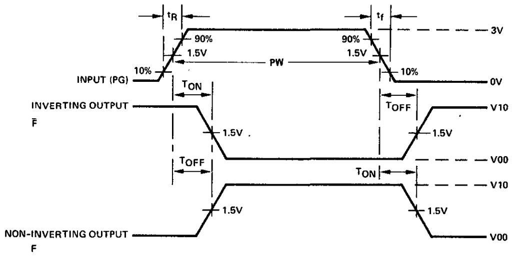
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds at 0.8V for logical "0" and 2.0V for logical "1".
11. All I_n data inputs are at 0V, V_{CC} = 5.25V.
12. Connect an external 1K resistor from V_{CC} to the output terminal for this test.

AC TEST FIGURE AND WAVEFORMS



INPUT PULSE:
PRR = 1 MHz
$t_R = t_f$ = 2.5 ns
PW = 50 ns

ALL DIODES ARE 1N3064
C_L INCLUDES PROBE & JIG CAPACITANCE



TEST TABLE														
TEST NO.	INPUTS												OUTPUTS	
	A_0	A_1	A_2	INH	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	E	F
1	PG	0	0	0	0	1	0	0	0	0	0	0	T	T
2	0	PG	0	0	0	0	1	0	0	0	0	0	T	
3	0	0	PG	0	0	0	0	0	1	0	0	0	T	
4	0	1	1	PG	0	0	0	0	0	1	0	0	T	
5	1	1	1	0	0	0	0	0	0	0	0	PG	T	

"1" = 2.7V "0" = GROUND

NOTE:
1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTHS FROM PACKAGE PINS.

2-INPUT 4-BIT DIGITAL MULTIPLEXER

82S33
82S34

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

These devices are 2-input, 4-Bit Digital Multiplexers designed for general purpose data-selection applications.

The 82S33 features non-inverting data paths; and, the 82S34 features inverting data paths.

The 82S34 has open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as forty four-bit words can be multiplexed by using twenty 82S34's in the WIRED-AND mode.

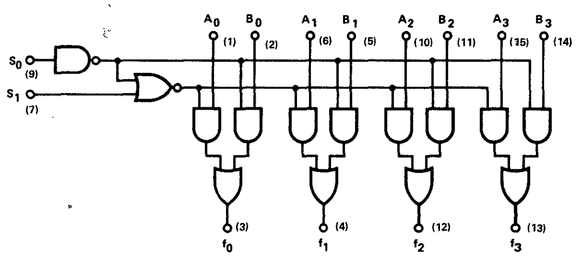
The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS (82S34)
- INHIBIT STATE

LOGIC DIAGRAM

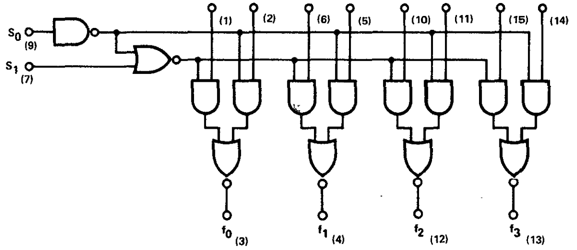
82S33



S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

82S34



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

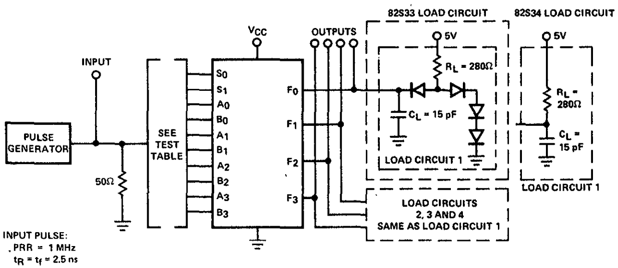
ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUTS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
"1" Output Voltage (82S33)	2.7			V	2.0V	2.0V	0.8V	0.8V	−1mA	
"0" Output Voltage (82S33)			0.5	V	0.8V	2.0V	2.0V	0.8V	20mA	
"0" Output Voltage (82S34)			0.5	V	0V	2.0V	0.8V	0.8V	20mA	
"1" Output Leakage Current (82S34)			250	µA	2.0V	2.0V	2.0V	2.0V	5.5V	
"0" Input Current (ALL)			400	µA	0.5V	0.5V	0.5V	0.5V		
"1" Input Current (ALL)			−10	µA	4.5V	4.5V	4.5V	4.5V		
Output Short Circuit Current (82S33)	−40		−100	mA	5V	5V	0V	0V	0V	
Input Clamp Voltage (ALL)			−1.2V	V	−18mA	−18mA	−18mA	−18mA		

$T_A = 25^oC$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUTS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
Power/Current Consumption:										
82S33			305/58	mW/mA		0V		0V		14
82S34			265/50	mW/mA		0V		0V		14
82S33/34 Turn-On/Turn-Off Times										
A_n, B_n to f_n			12	ns						8,13
S_0 to f_n			20	ns						8,13
S_1 to f_n			18	ns						8,13

AC TEST FIGURE AND WAVEFORMS

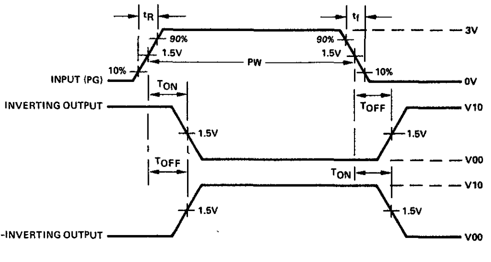


INPUT PULSE:
PRR = 1 MHz
$t_R = t_f = 2.5$ ns
PW = 50 ns

ALL DIODES ARE 1N3064
C_L INCLUDES PROBE & JIG CAPACITANCE

TEST TABLE														
TEST NO.	INPUTS										OUTPUTS			
	S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	PG	0	1	0	1	0	1	0	1	0	T			
2	PG	0	1	0	1	0	1	0	1	0	T	T	T	T
3	PG	0	0	1	0	1	0	1	0	1		T		
4	1	PG	1	0	1	0	1	0	1	0			T	
5	0	0	0	PG	0	0	0	0	0	0	T			
6	0	1	0	0	0	PG	0	0	0	0		T		
7	1	0	0	0	0	0	PG	0	0	0			T	
8	1	0	0	0	0	0	0	0	PG	0				T

"1" = 2.7V "0" = GROUND



NOTE:
1. A.C. TEST JIG'S MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIG'S MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

QUAD EXCLUSIVE-OR ELEMENT | 82S41

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

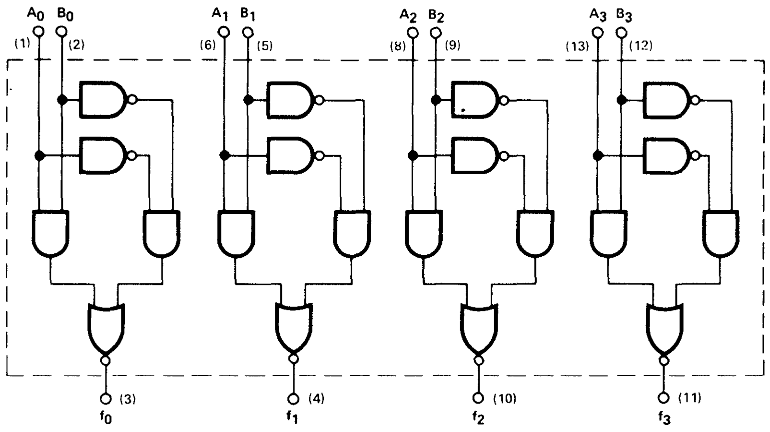
The 82S41 contains four independent gating structures to perform the Exclusive-OR function on two input variables. The output of the 82S41 employs the totem-pole structure characteristic of TTL devices.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS

LOGIC DIAGRAMS

82S41 QUAD EXCLUSIVE–OR



A	B	f
0	0	0
1	0	1
0	1	1
1	1	0

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

NOTE: Pin-Out for Dual In-Line Package Only

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
					INPUTS		OUTPUTS	
	MIN.	TYP	MAX	UNITS	A	B		
Output "1" Voltage	2.7			V	2.0V	0.8V	−1mA	
Output "0" Voltage			0.5	V	2.0V	2.0V	20mA	
Input "1" Current			10	μA	4.5V	4.5V		11
Input "0" Current			−800	μA	0.5V	0.5V		12
Power/Current Consumption			290/55	mW/mA				13
Output Short Circuit Current	−40		−100	mA		−18mA	0V	13
Input Clamp Voltage	−1.2			V	−18mA			

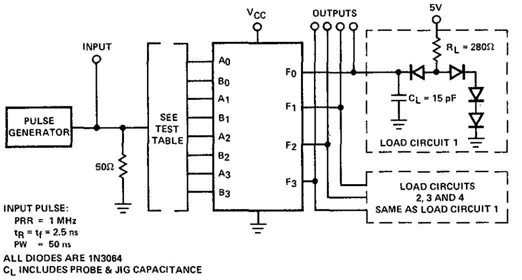
$T_A = 25^oC$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
					INPUTS			
	MIN	TYP	MAX	UNITS	A	B	OUTPUTS	
Turn-On/Turn-Off Times			10	ns				9

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. Manufacturers reserves the right to make design and process changes and improvements.
11. A and B are tested separately. When A is 4.5V, B is 0V, and vice versa.
12. A and B are tested separately. When A is 0.4V, B is 5.25V, and vice versa.
13. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS

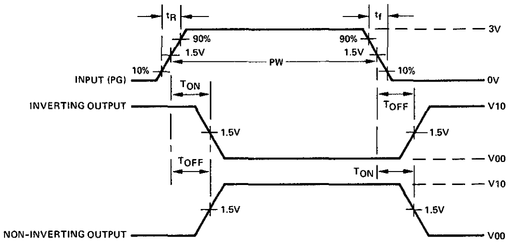


TEST TABLE												
TEST NO.	INPUTS								OUTPUTS			
	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	0	0	0	PG	0	0	0	0		T		
2	0	PG	0	0	0	0	0	0	T			
3	0	0	0	PG	0	0	0	0		T		
4	0	0	0	0	0	PG	0	0			T	
5	0	0	0	0	0	0	0	PG				T
6	PG	0	0	0	0	0	0	0	T			
7	0	0	0	0	0	0	PG	0				T

"1" = 2.7V "0" = GROUND

NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.



BINARY-TO-OCTAL DECODER
BCD-TO-DECIMAL DECODER

82S50
82S52

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S50 and 82S52 are gate arrays for decoding and logic conversion applications.

The 82S50 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

The 82S52 converts a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

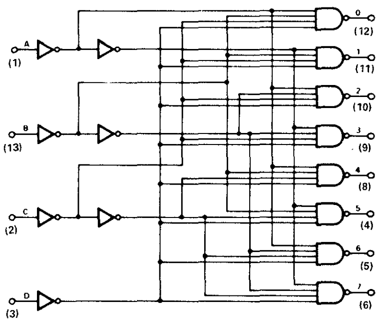
The 82S52 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs. The selected output is a logic "0".

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- INHIBIT INPUT FORCES ALL OUTPUTS HIGH (82S50)
- 82S52 CAN REPLACE 9301 FOR HIGHER SPEED

LOGIC DIAGRAMS

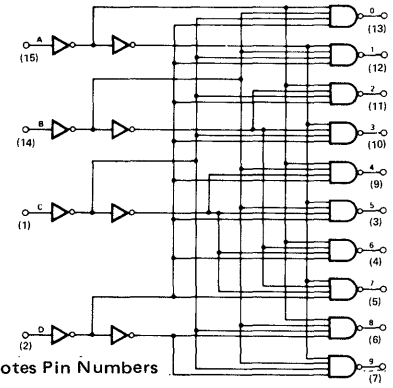
82S50



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

*NOTE: PIN-OUT FOR DUAL IN-LINE PACKAGE ONLY

82S52



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

*NOTE: PIN-OUT FOR DUAL IN-LINE PACKAGE ONLY

TRUTH TABLE

INPUT STATE				OUTPUT STATES									
				82S50								82S52	
A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS						
"1" Output Voltage	2.7			V					−1mA	10
"0" Output Voltage			0.5	V					20mA	10
"1" Input Current A, B, C, D			10	μA	4.5V	4.5V	4.5V	4.5V		
"0" Input Current (ALL)			−400μA	mA	0.5V	0.5V	0.5V	0.5V		

T_A = 25°C and V_{CC} = 5.0V

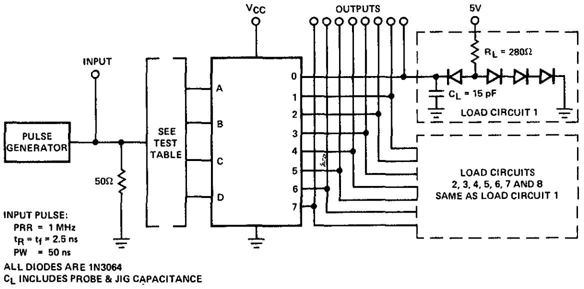
CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS						
Turn-on Delay t_{on}			16	ns						8
Turn-off Delay t_{off}			16	ns						8
Power/Current Consumption										
(82S50 Only)			380/72	mW/mA	5.25V	5.25V	5.25V	0V		11
(82S52 Only)			450/85	mW/mA						
Input Clamp Voltage			−1.2	V	−18mA	−18mA	−18mA	−18mA		
Output Short Circuit Current (ALL)	−40		−100		4.0V	4.0V	4.0V	4.0V	0V	11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1". "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Inputs for "1" and "0" output voltage test is per TRUTH table with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS

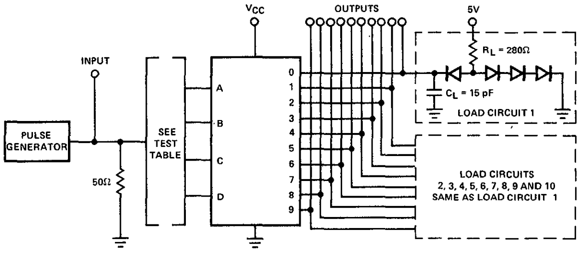
82S50



TEST TABLE												
TEST	INPUTS				OUTPUTS							
NO.	A	B	C	D	0	1	2	3	4	5	6	7
1	1	1	PG	0								T
2	1	1	PG	0				T				T
3	PG	1	0	0			T	T				
4	0	PG	1	0					T		T	
5	0	0	0	PG	T							
6	1	0	PG	0		T				T		

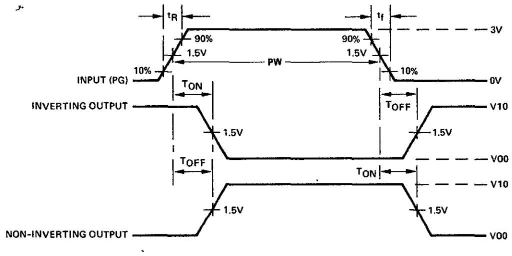
"1" = 2.7V "0" = GROUND

82S52



TEST TABLE														
TEST	INPUTS				OUTPUTS									
NO.	A	B	C	D	0	1	2	3	4	5	6	7	8	9
1	0	0	PG	0					T					
2	PG	1	0	0			T	T						
3	0	0	0	PG	T								T	
4	1	0	PG	0		T				T				
5	1	PG	0	1										T
6	PG	1	1	0										

"1" = 2.7V "0" = GROUND



NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

9-BIT PARITY GENERATOR AND CHECKER

82S62

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S62 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 82S62. (A logic 1 on the INHIBIT input forces both outputs to a logic 0.)

When used as a Parity Generator, the 82S62 supplies a parity bit which is transmitted together with the data word.

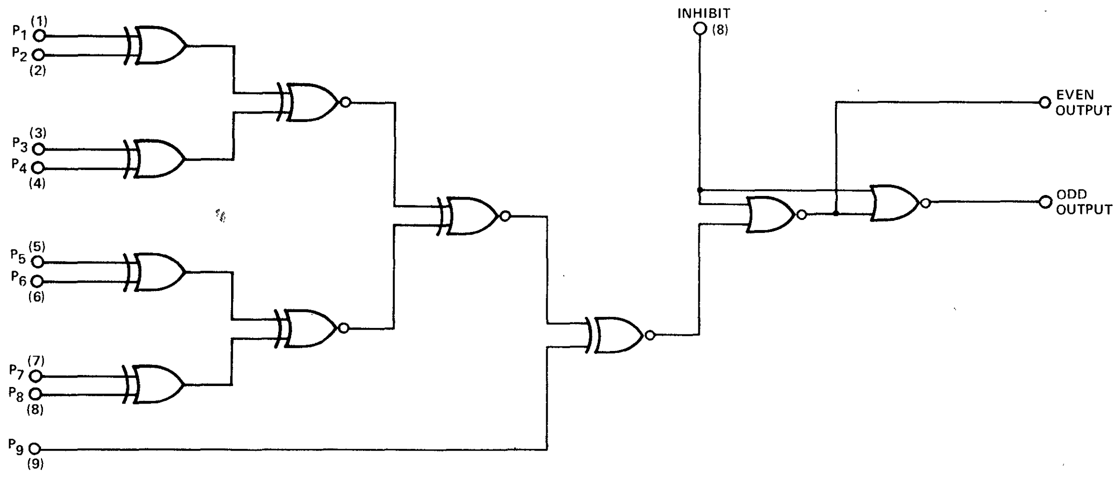
At the receiving end, the 82S62 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- EVEN/ODD PARITY OUTPUTS
- INHIBIT INPUT
- PNP INPUTS

LOGIC DIAGRAM

82S62



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

LOGIC EQUATIONS:

Odd =

$\underline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

Even =

$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

NOTE: Pin-Outs shown for Dual In-Line package only

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN	TYP	MAX	UNITS	DATA INPUT UNDER TEST			
"1" Output Voltage								
Even	2.7			V	0V	.8V	–1mA	
Odd	2.7			V	2.0V	.8V	–1mA	
"0" Output Voltage								
Even			0.50	V	2.0V	.8V	20mA	
Odd			0.50	V	0V	.8V	20mA	
"0" Input Current								
Data Inputs P_1–P_8			–800	µA	0.5V			
Data Input P_9			–1.2	mA	0.5V			
Inhibit			–800	µA		0.5V		
"1" Input Current								
Data Inputs			10	µA	4.5V			
Inhibit			10	µA		4.5V		
Power/Current Consumption			355/67	mW/mA				11
Output Short Circuit Current	–40		–100					
Even	–40		–100	mA	0V	0V	0V	11
Odd	–40		–100	mA	4.0V	0V	0V	11

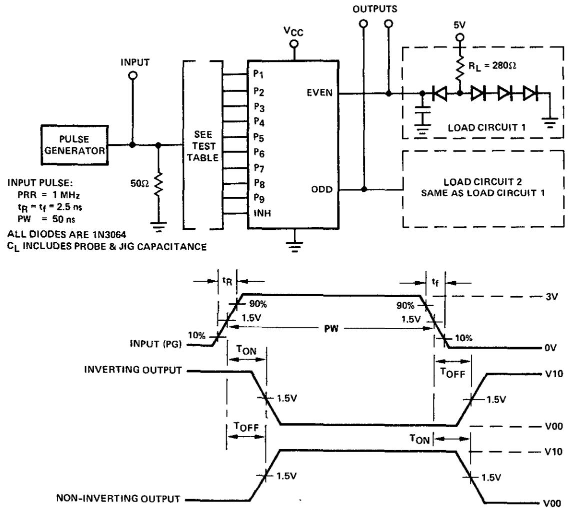
T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN	TYP	MAX	UNITS	UNDER TEST			
Turn-on/Turn-off Times								
P_1 – P_8 to Even			23	ns	Pulse			8
P_1 – P_8 to Odd			28	ns	Pulse			8
P_9 to Even			12	ns	Pulse			8
P_9 to Odd			18	ns	Pulse			8
Inhibit to Even			9	ns		Pulse		8
Inhibit to Odd			9	ns		Pulse		8

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
11. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



TEST TABLE												
TEST NO.	INPUTS										OUTPUTS	
	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	INH	EVEN	ODD
1	PG	0	0	0	0	0	0	0	0	0		T
2	PG	0	0	0	0	0	0	0	0	0	T	T
3	0	0	PG	0	0	0	0	0	0	0	T	T
4	0	0	0	0	PG	0	0	0	0	0	T	T
5	0	0	0	0	0	0	PG	0	0	0	T	T
6	0	0	0	0	0	0	0	0	PG	0	T	T
7	0	0	0	0	0	0	0	0	0	PG	T	T

"1" = 2.7V "0" = GROUND

NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

2-INPUT, 4-BIT DIGITAL MULTIPLEXER

82S66
82S67

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S66/82S67 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing Schottky TTL circuit structures. The 82S67 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

The multiplexer is able to choose from two different input sources, each containing 4 bits: $A = (A_0, A_1, A_2, A_3)$, $B = (B_0, B_1, B_2, B_3)$. The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

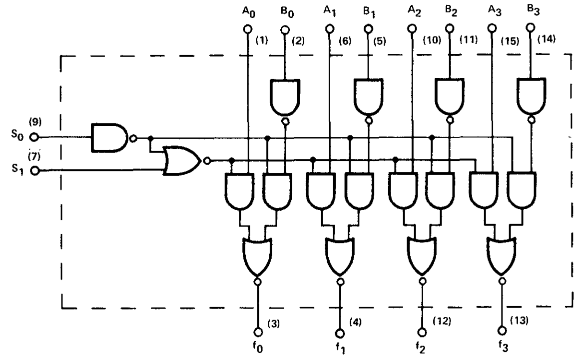
For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with adder elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS (82S67)
- INHIBIT STATE

LOGIC DIAGRAM AND TRUTH TABLE

82S66/82S67



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\bar{A}_n$
1	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
"1" Output Voltage (82S66)	2.7	3.5		V	0.8V	2.0V	0.8V	0.8V	−1mA	
"0" Output Voltage			0.5	V	2.0V	2.0V	2.0V	0.8V	20mA	
"1" Output Leakage Current (82S67)			250	μA	0.8V	2.0V	2.0V	0.8V	5.5V	
"0" Input Current										
A_n, B_n			−400	μA	0.5V	0.5V	0V	0V		
S_0, S_1			−400	μA			0.5V	0.5V		
"1" Input Current										
A_n, B_n			10	μA	4.5V	4.5V		2.0V		
S_0, S_1			10	μA			4.5V	4.5V		
Output Short Circuit Current (82S66)	−40		−100	mA						12

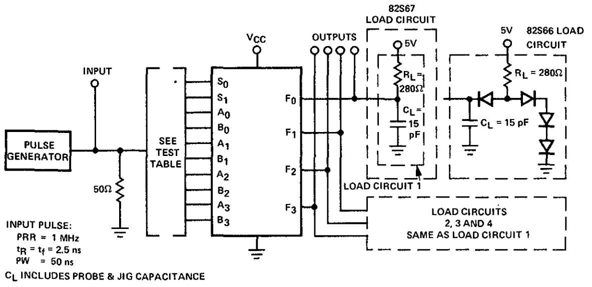
$T_A = 25^oC$ and $V_{CC} = 5.0V$

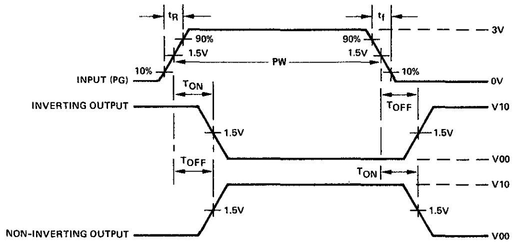
CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
Turn-on/Turn-off Times (82S66)										
S_1 to f_n			15	ns						9
S_0 to f_n			18	ns						9
A_n to f_n			10	ns						9
B_n to f_n			12	ns						9
Propagation Delay (82S67)										
S_1 to f_n			18	ns						9
S_0 to f_n			20							
A_n to f_n			12	ns						9
B_n to f_n			15	ns						9
Power/Current Consumption			365/69	mW/mA	4.5V	0V	4.5V	0V		12

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. V_{CC} = 5.25 V.

AC TEST FIGURE AND WAVEFORMS





TEST TABLE

TEST NO.	INPUTS										OUTPUTS			
	S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	1	PG	1	1	1	1	1	1	1	1	T			
2	1	PG	1	1	1	1	1	1	1	1	T	T	T	T
3	PG	0	1	1	1	1	1	1	1	1	T			T
4	0	0	0	0	0	PG	0	0	0	0		T		
5	0	0	0	0	0	0	0	PG	0	0			T	
6	1	0	PG	1	0	1	0	1	0	1	T			
7	1	0	0	1	0	1	0	1	PG	1				T

"1" = 2.7V "0" = OUTPUT

NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

8-INPUT DIGITAL MULTIPLEXER

82S31
82S32

ADVANCED INFORMATION

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 82S31 is a variation of the 82S30 that provides open collector output $\overline{f}$ for expansion of input terms. The 82S32 is similar to the 82S30 except in the effect of the INHIBIT input on the $\overline{f}$ output. With the INHIBIT low, the selected input appears at the f output and, in complement, on the $\overline{f}$ output. With the INHIBIT input high, both the f and the $\overline{f}$ output are unconditionally low.

FEATURES

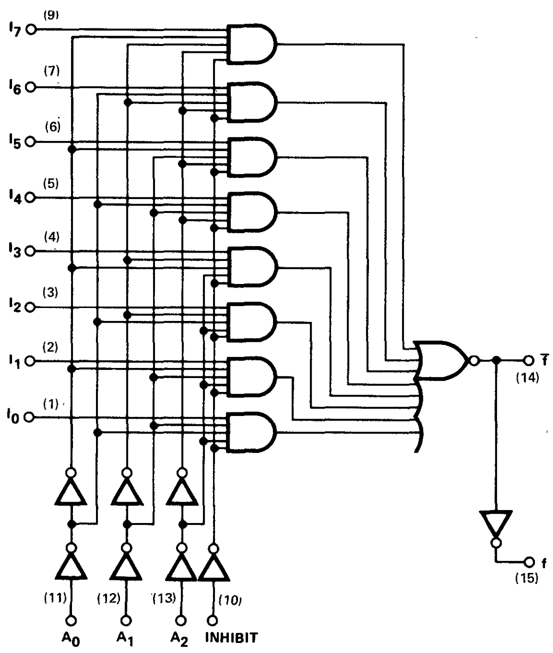
- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUT (82S31)
- DIRECT OUTPUT INHIBIT (82S32)

ELECTRICAL CHARACTERISTICS

Propagation Delay (Typ)		
	82S32	82S31
A_n to $\overline{f}$	12ns	14ns
I_n to $\overline{f}$	7ns	9ns
Input Load Current (Max)		
I_{in}"0"		400µA
I_{in}"1"		10µA
Output Current		
I_{out}"0"		20mA @ 0.5V
I_{out}"1"		1mA @ 2.7V (82S30/32)

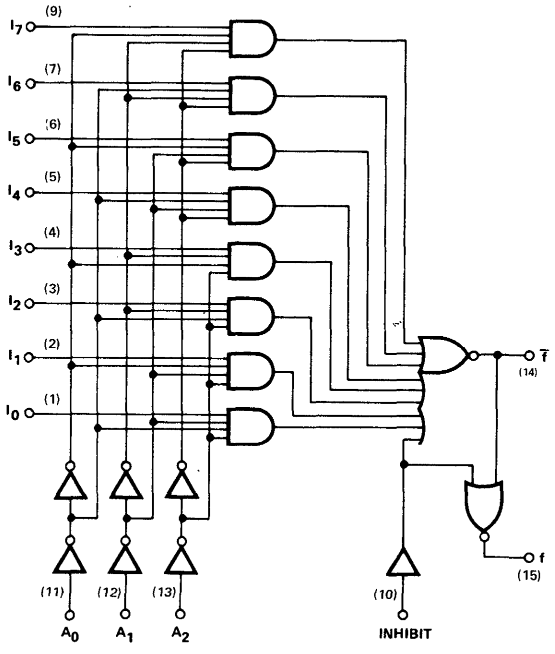
LOGIC DIAGRAMS

82S31



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers
*82S31 has Open Collector

82S32



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

82S42 4-BIT QUAD EXCLUSIVE-NOR

ADVANCED INFORMATION

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S42 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 82S42 outputs are bare collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

FEATURES

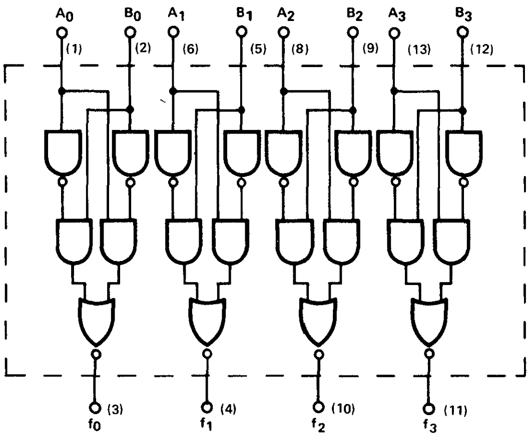
- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS

ELECTRICAL CHARACTERISTICS

Propagation Delay (Typ)	
A_n, B_n to f_n	9ns (82S42)
Input Load Current (Max)	
I_{In}"0"	800μA
I_{In}"1"	20μA
Output Current (Min)	
I_{out}"0"	30mA @ 0.5V (82S42)

LOGIC DIAGRAM

82S42 QUAD EXCLUSIVE–NOR



A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

4-BIT SHIFT REGISTERS

82S70
82S71

ADVANCED INFORMATION

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S70 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control.

The 82S71 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 82S70 element.

FEATURES

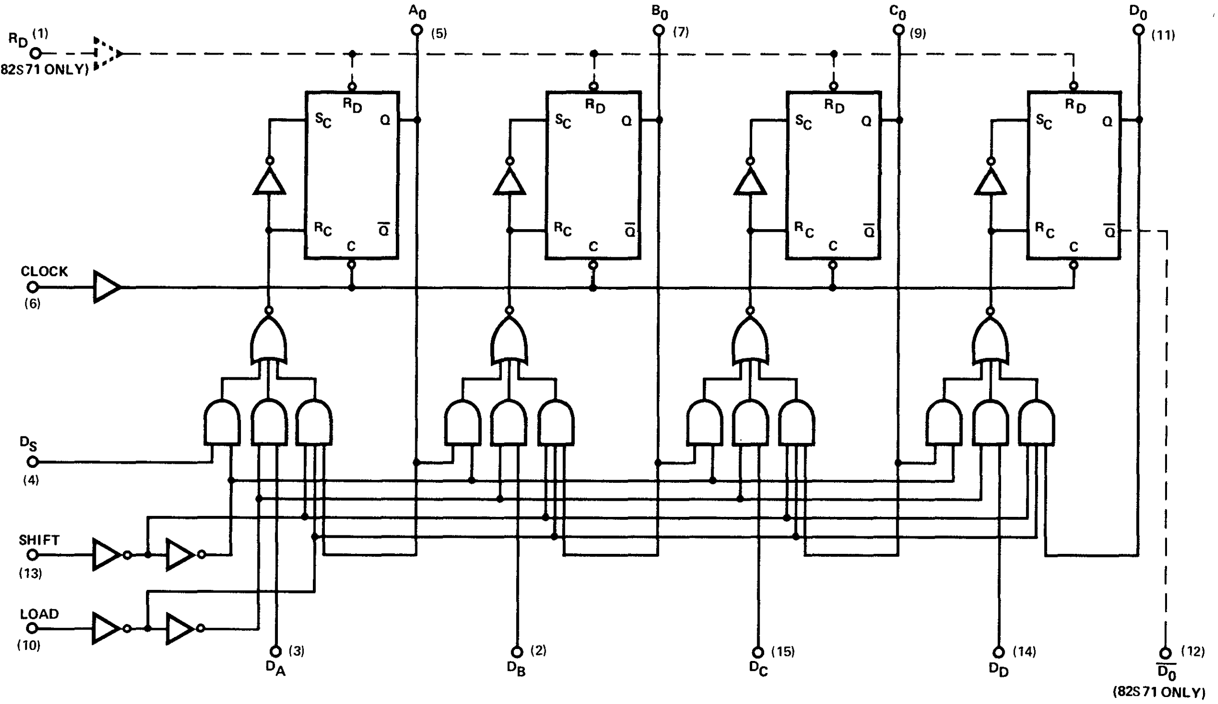
- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- SYNCHRONOUS LOAD
- SHIFT RIGHT/LEFT CAPABILITY
- HOLD MODE

ELECTRICAL CHARACTERISTICS

Transfer Rate	60 MHz (Typ)
Input Load Current (Max)	
I_{in}"0"	400μA
I_{in}"1"	25μA
Output Current	
I_{out}"0"	20mA @ 0.5V
I_{out}"1"	1mA @ 2.7V

LOGIC DIAGRAM

82S70 AND 82S71



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

82S90 82S91 PRESETTABLE HIGH SPEED DECADE/BINARY COUNTER

ADVANCED INFORMATION

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S90 Decade Counter and 82S91 Binary Counter are high speed devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 82S91 Binary Counter may be connected as a divide-by-two; four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- CLOCK FREQUENCY = 100 MHz (Typ)
- PARALLEL LOAD CAPABILITY
- ASYNCHRONOUS RESET

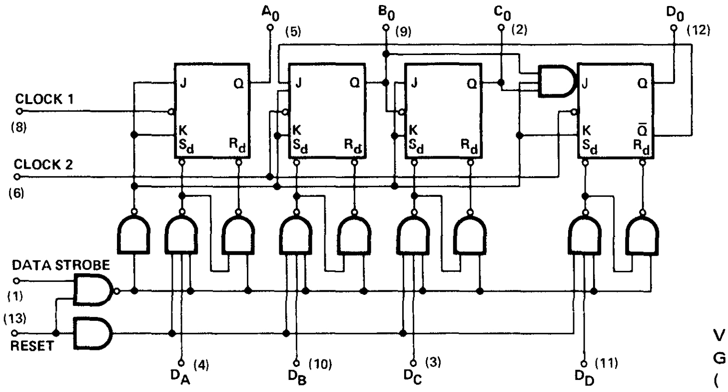
ELECTRICAL CHARACTERISTICS

Clock Frequency	100 MHz (Typ)
Strobe/Reset Hold Time	10ns (Typ)
Output Current (Min)	
I_{out}"0"	20mA @ 0.5V
I_{out}"1"	1mA @ 2.7V

LOGIC DIAGRAMS AND TRUTH TABLES

82S90

Bi-Quinary (5-2)				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	1	1	0
4	0	0	0	1
5	1	0	0	0
6	1	1	0	0
7	1	0	1	0
8	1	1	1	0
9	1	0	0	1

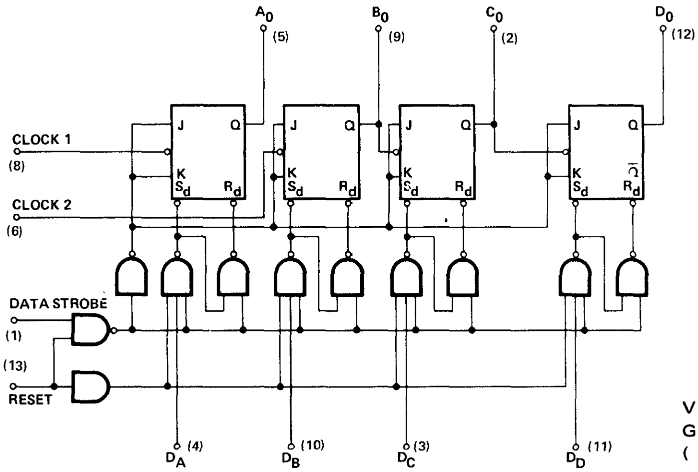


Decade (BCD)				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

82S91

Binary				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

SECTION 8
BIPOLAR MEMORIES

2048 BIT BIPOLAR ROM (256x8 ROM)
4096 BIT BIPOLAR ROM (512x8 ROM)

8204
8205

THIS PRODUCT AVAILABLE IN 0°C TO 75°C TEMPERATURE RANGE ONLY

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8205 and 8204 are high performance bipolar ROM's incorporating the storage output or memory data register into the chip. Data is addressed by applying address information to the address lines. After valid data appears at the output of the memory array, (typically 35ns after the address is applied) and if the circuit is enabled, the strobe pulse will enter data into the 8 bit output latch register. A D-type latch (L) is used to enable the tri-state output drivers. If the circuit enable signals are valid, the strobe will set the latch. This turns on the output stage. The latch will remain set and keep the output enabled until the chip is disabled and the next strobe pulse occurs. If the strobe line is held high, the ROM will function in a conventional mode. The output will be controlled solely by the chip enable and the output latches will be bypassed.

See page 241 for ASCII (ADDRESS) to EBCDIC (DATA) and EBCDIC (ADDRESS) to ASCII (DATA) and 246/248 for ORDERING BLANKS.

FEATURES

- MICROPROGRAMMING
- HARDWIRE ALGORITHMS
- CHARACTER GENERATION
- CONTROL STORE

APPLICATIONS

BUFFERED ADDRESS LINES

ON THE CHIP DECODING

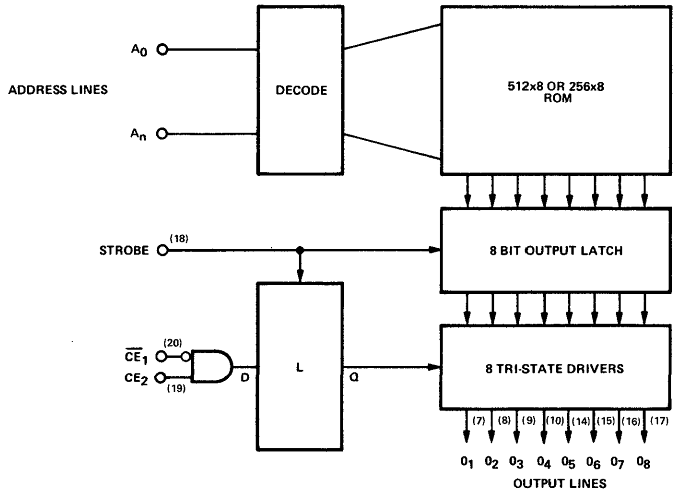
ON THE CHIP STORAGE LATCHES

TRI-STATE OUTPUT

PROTECTED INPUTS

BLOCK DIAGRAM

256 x 8 AND 512 x 8 MEMORY ORGANIZATION



Address Pins	8204	8205
A_0	(21)	(20)
A_1	(22)	(21)
A_2	(23)	(23)
A_3	(1)	(1)
A_4	(2)	(2)
A_5	(4)	(3)
A_6	(5)	(4)
A_7	(6)	(5)
A_8	–	(6)

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Input "0" Current			–100	µA	$V_{in} = 0.5V$	
Input "1" Current			25	µA	$V_{in} = 5.25V$	
Input (0) Threshold Voltage	0.85			V		
Input (1) Threshold Voltage		2		V		
Input Clamp Voltage	–1.0			V	$I_{in} = -5.0mA$	
Output (0) Current		0.2	0.5	V	$I_{out} = 9.6$ mA	
Output (1) Current	2.7	3.3		V	$I_{out} = -2.0mA$	
Output (1) Short Circuit Current	–20	–35	–70	mA	$V_{out} = 0V$, $V_{CC} = 5.0V$	2
Input Capacitance		5		pF	$V_{IH} = 2.0V$, $V_{CC} = 5.0V$	
Output Capacitance		8		pF	$V_{out} = 2.0V$; $V_{CC} = 5.0V$	5
Power Supply Current		135	170	mA	$V_{CC} = 5.0V$	
Output (1) off Leakage Current (Chip Disabled)			100	µA	$V_{in} = 2.7V$	
Output (0) off Leakage Current (Chip Disabled)			–100	µA	$V_{in} = 0.5V$	

T_A = 25°C and V_{CC} = 5.0V

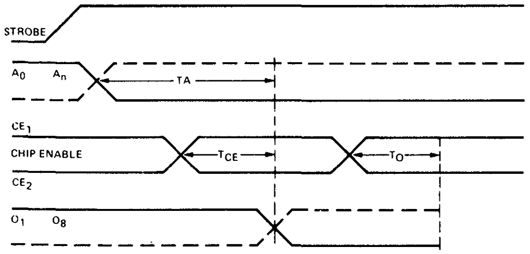
CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Address Access Time T_A		35	60	ns	Read Mode I or Read Mode II	6
Address Hold Time T_{ADS}	0	-10		ns	Read Mode 2 Only	6
Chip Enable Access Time T_{CE}		20	45	ns	Read Mode I or Read Mode II	6
Chip Enable Hold Time T_{CDS}	12	5		ns	Read Mode II Only	6
Output Disable Time T_O		20	45	ns	Read Mode I or Read Mode II	6
Strobe Pulse Width T_{SW}	33	20		ns	Read Mode II Only	6
Strobe Set-Up Time T_S		30	60	ns	Read Mode II Only	6
Output Disable Time T_R		18	32	ns	Read Mode I Only	6

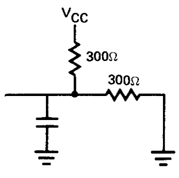
NOTES:

1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 5.5V.
   Input currents must not exceed ±30 mA.
   Output currents must not exceed ±100 mA.
   Storage temperature must be between -60°C to +150°C.
5. Chip disabled.
6. Rise and fall times for tests must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

MEMORY TIMING

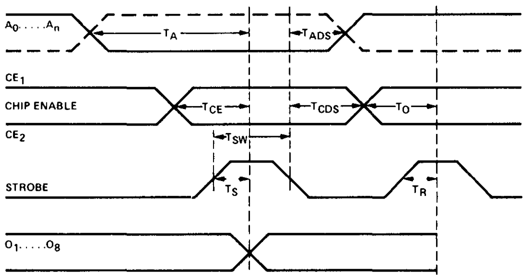
READ MODE I (OUTPUT LATCHES NOT USED)

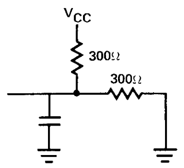




If the strobe is high, the device functions in a manner identical to conventional bipolar ROM's. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_O is the time required to disable the output and switch it to an 'off' or high impedance state after it has been enabled.

READ MODE II (OUTPUT LATCHES USED)





In Read Mode II, the address is applied to the memory element T_A ns before output details desired. Applying the chip enable does not directly enable the outputs. When the strobe is applied T_S nanoseconds before the output, data from the memory array is copied into the output latches and the chip enable signal is copied into the delay latch L. The latch L in turn enables the output. After the strobe reaches the strobe level, both the chip enable and address lines may be altered but the output data stored in the latches will remain unchanged and the output of the circuit will remain enabled. The output will stay enabled until another strobe copies a Not chip enable signal into the latch L. The switching of the output to the "off" or high impedance state occurs T_R nanoseconds after the strobe.

8-BIT CONTENT ADDRESSABLE MEMORY (4x2 CAM) 8220

PRODUCT AVAILABLE IN 0°C TO 75°C TEMPERATURE ONLY

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8220 CAM Element is a high speed monolithic array, incorporating the necessary addressing logic and eight identical memory cells organized as four words, each being two bits long. In reference to data-in/data-stored, the 8220 can be conditioned to perform the following functions: associate, write-in only, and read-out only.

When addressed into the "ASSOCIATE" mode, this element offers the novel capability of data association, where each cell (M_{nj}) will respond with a "Match" or "Mismatch" answer (Y_n) to each bit presented to the data inputs (I_j), depending on presence or absence of an alike bit stored within the cell.

Write-in can be simultaneously done to all bits, or one bit at a time. Read-out of stored information is performed on one word at a time. Cell-selection for read and write is performed by proper addressing of Y_n and A_n lines.

The element's output structures (Y_n and D_j) are of the "bare collector" variety and can be mutually connected, thus allowing direct expansion when multiple packages are employed. Expansion of the CAM may be implemented in both directions, i.e., in the word length and in the number of words.

The CAM circuit structure is the familiar TTL type (DCL Family) and fully compatible with TTL and DTL input/output structures.

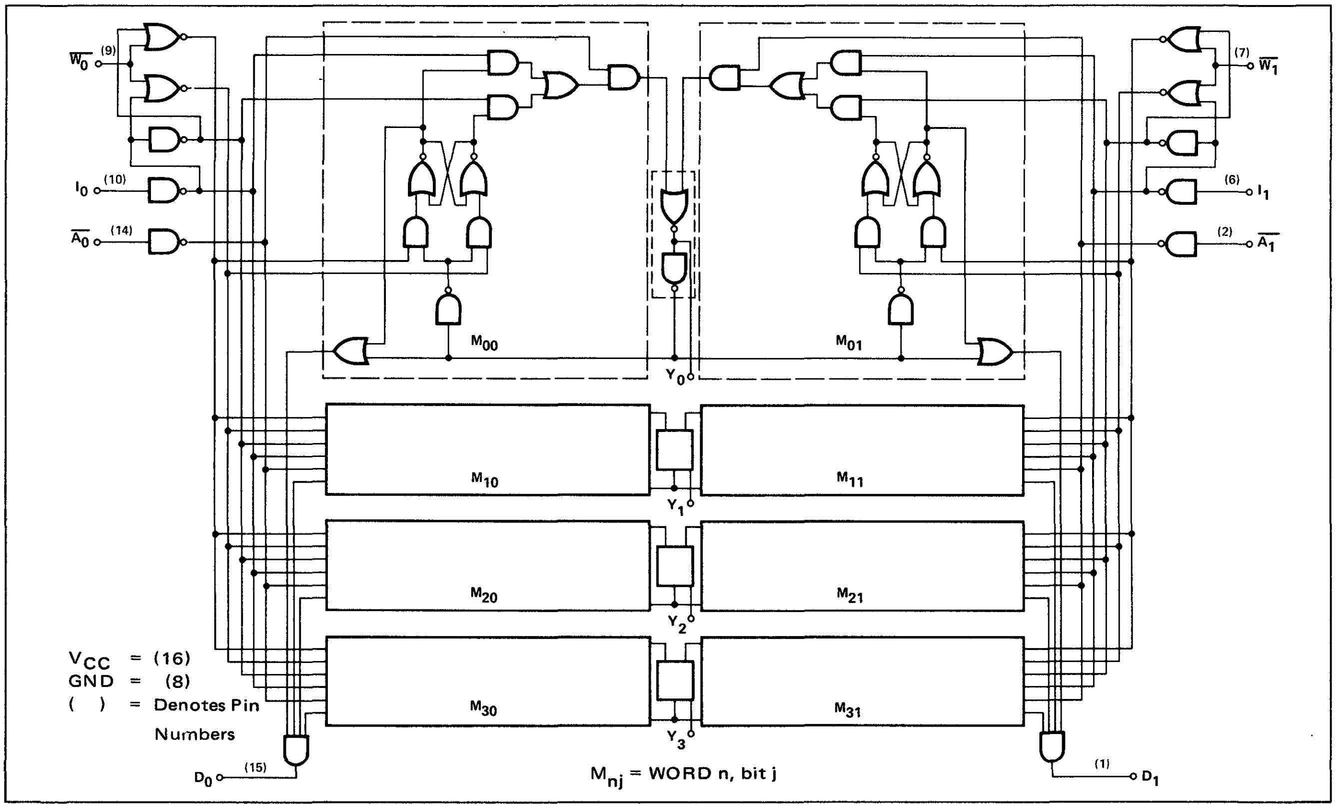
FEATURES

- WRITE ENABLE CONTROL LINES
- ASSOCIATE CONTROL LINES
- ADDRESS SELECT CONTROL LINES
- ASSOCIATES IN 20nsec TYP.
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

DATA-TO-MEMORY COMPARISON
PATTERN RECOGNITION
HIGH SPEED INFORMATION RETRIEVAL
CACHE MEMORY
AUTO CORRELATION
VIRTUAL MEMORY
LEARNING MEMORY

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				$\overline{Wj}$	$\overline{Aj}$	I_j	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
"0" Output Voltage											
Yn			0.4	V	2.0V	0.8V	2.0V	30mA			8, 9
			0.6	V	2.0V	0.8V	2.0V	60mA			
Dj			0.4	V	2.0V	2.0V			0.8V	20mA	8, 9
			0.6	V	2.0V	2.0V			0.8V	40mA	
"1" Output Leakage Current											
Yn			125	µA		2.0V					10
Dj			100	µA				0V	0V		10
"1" Input Current											
Ij and $\overline{A}_j$			40	µA		4.5V	4.5V				
$\overline{Wj}$			80	µA	4.5V						
"0" Input Current											
Ij, Yn and $\overline{Aj}$	-0.1		-1.2	mA		0.4V	0.4V	0.4V			

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				Wj	Aj	Tj	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
Delay Time											
Associate ($\overline{Aj}$ to Yn)		20	30	ns							8, 11
Associate (Ij to Yn)		35	45	ns							8, 11
Read-Out (Yn to Dj)		30	40	ns							8, 11
Write-In to Read-Out ($\overline{Wj}$ to Dj)		45	60	ns							
Write Pulse Width		20	35	ns							
Power Consumption			590/ 118	mW/mA							

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Prior to this test write in a "0" in all or desired Memory cells as follows: Wj = Ij = 0V, Aj = V_{CC}.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Connect an external 1K ohm + 1% resistor from V_{CC} to the output terminal for this test.
11. See AC test Figures on the following pages.

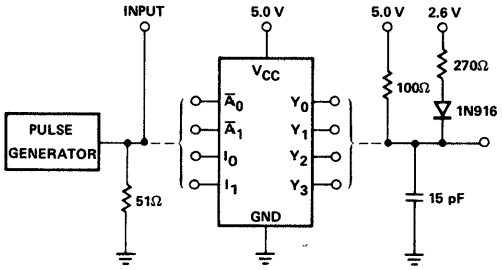
MODE OF OPERATION

FUNCTION	$\overline{W}_0$ $\overline{W}_1$ $\overline{A}_0$ $\overline{A}_1$ I_0 I_1	REMARKS (Ref. Definitions & Glossary)
HOLD	1 1 1 1 x x	NO OPERATION
ASSOCIATE	1 1 1 0 x x	Question / Answer / Output State ? $I_1=M_{i1}$ – YES — $Y_i=1$, $Y_k=0$ – NO — $Y_i=Y_k=0$
	1 1 0 1 x x	? $I_0=M_{i0}$ – YES — $Y_i=1$, $Y_k=0$ – NO — $Y_i=Y_k=0$
	1 1 0 0 x x	$I_1=M_{i1}$ and $I_0=M_{i0}$? – YES — $Y_i=1$, $Y_k=0$ – NO — $Y_i=Y_k=0$

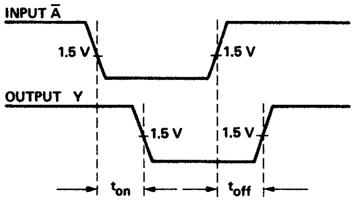
FUNCTION	$\overline{W}_0$ $\overline{W}_1$ $\overline{A}_0$ $\overline{A}_1$ I_0 I_1	Forced Y_i	Forced Y_k	REMARKS (Ref. Definitions & Glossary)
HOLD	1 1 1 1 x x			NO OPERATION
WRITE-IN	1 0 1 1 x x	1	0	WRITE I_1 into M_{i1}
	0 1 1 1 x x	1	0	WRITE I_0 into M_{i0}
	0 0 1 1 x x	1	0	WRITE I_1 and I_0 into M_{i1} and M_{i0}
READ-OUT	1 1 1 1 x x	1	0	$D_0=$ 1 - IF $M_{i0}=1$ 0 - IF $M_{i0}=0$
	1 1 1 1 x x	1	0	$D_1=$ 1 - IF $M_{i1}=1$ 0 - IF $M_{i1}=0$
	1 1 1 1 x x	0	0	$D_0=D_1=1$

AC TEST FIGURES AND WAVEFORMS

ASSOCIATE DELAY AND INPUT DELAY



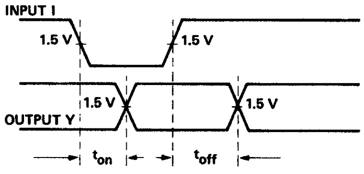
ASSOCIATE DELAY



NOTES:

1. When checking $\overline{A_0}$ let $\overline{A_1}$ = "1" and when checking $\overline{A_1}$ let $\overline{A_0}$ = "1".
2. $\overline{W_0}$ = $\overline{W_1}$. = "1".

INPUT DELAY

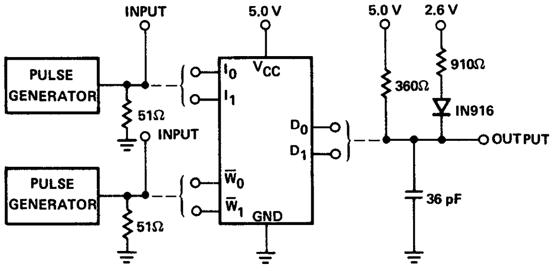


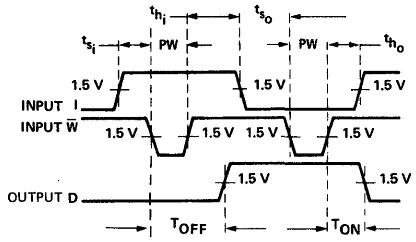
NOTES:

1. When checking I_1, $\overline{A_1}$ = "0" and $\overline{A_0}$ = "1" and when checking I_0, $\overline{A_0}$ = "0" and $\overline{A_1}$ = "1"
2. $\overline{W_0}=\overline{W_1}$ = "1".

AC TEST FIGURES AND WAVEFORMS (Cont'd)

WRITE DELAY

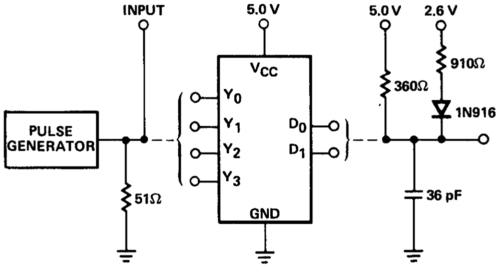


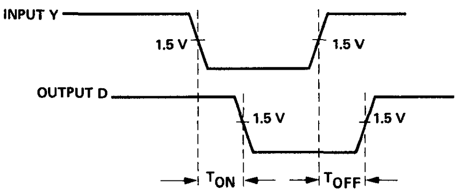


t_{s_i} = "1" set-up time.
t_{s_o} = "0" set-up time.
th_i = "1" hold time.
th_o = "0" hold time.
PW = Pulse width

NOTES:
1. $\overline{A}_0 = \overline{A}_1$ = "1".
2. Let all non-selected Y's = "0".
3. W's pulse width is 40ns @50% points.

READ DELAY





NOTES:
1. A tested bit must store a "0".
2. $\overline{W}_0 = \overline{W}_1$ = "1".
3. $\overline{A}_0 = \overline{A}_1$ = "1".
4. All non-tested Y's = "0".

GENERAL NOTES FOR AC TESTING:
1. Use 5k Probes for all AC tests TEK 169 or equivalent.
2. The Pulse Generator signal should consist of the following
   Frequency: 10 MHz ±5 MHz
   Amplitude: 0V to 3V
   Rise & Fall Times: 5 ns ±2ns
3. i = bit number (i = 0, 1). j = word number (j = 0, 1, 2, 3).

INPUT/OUTPUT DEFINITIONS

I_j – Data Inputs
Data entering these terminals are either compared with stored information at the cell(s) in the "associate" mode or stored in the cell(s) in the "write-in" mode.

$\overline{A}_j$ – Associate Controls
A logical "0" at this pin enables Data-Cell association to result into a defined logical level at the Y_n lines (e.g. Y_n = "1" = Match, Y_n = "0" Mismatch). A logical "1" at this pin forces all Y_n to a "1".

$\overline{W}_j$ – Write Enable
A logical "0" at this control pin opens the gates of the selected word, allowing data-in to be stored. A logical "1" locks the gates such that data-in can no longer disturb the cell(s).

Y_n – "Associate" Output and Address Selection Control
During "Associate" mode these "bare collector" lines provide output results of match or mismatch between input and stored data (logical "1" = Match, logical "0" = Mismatch).

In the read and write modes these terminals act as input controls and word-select lines Y lines (Y_1) associated with words desired to accept writing of data or read-out are to be kept in the logical "1" state and the remaining Y lines (Y_k) to be forced to a logical "0" state. (Note that A = 1 forces all Y_n = 1).

D_j – Data Output
These are "bare collector" output lines indicating the state of one or more selected cells. Cell-Selection is accomplished as defined under "Y_n" above.

GLOSSARY OF TERMS – SUBSCRIPTS

A.
n = Word number = 0, 1, 2 and 3
j = Bit number = 0 or 1
i = Input/Output number(s) associated with cell(s) upon which a "Write-in", "Read-out" or other function is being performed.
k = Input/Output number(s) other than "i" above.
M = Designation of Memory Cell (word) = eight identical cells in each package.

B. Examples
1. I_j for bit "1" equals I_1.
2. $M_{nj} = M_{10}$ = word "1" bit "0".
3. Y_i = 0, Y_k = 1: for i = words 1 and 3; then k = words 0 and 2: $Y_{1,3}$ = 0 and $Y_{0,2}$ = 1.

APPLICATION: LEARNING MEMORY

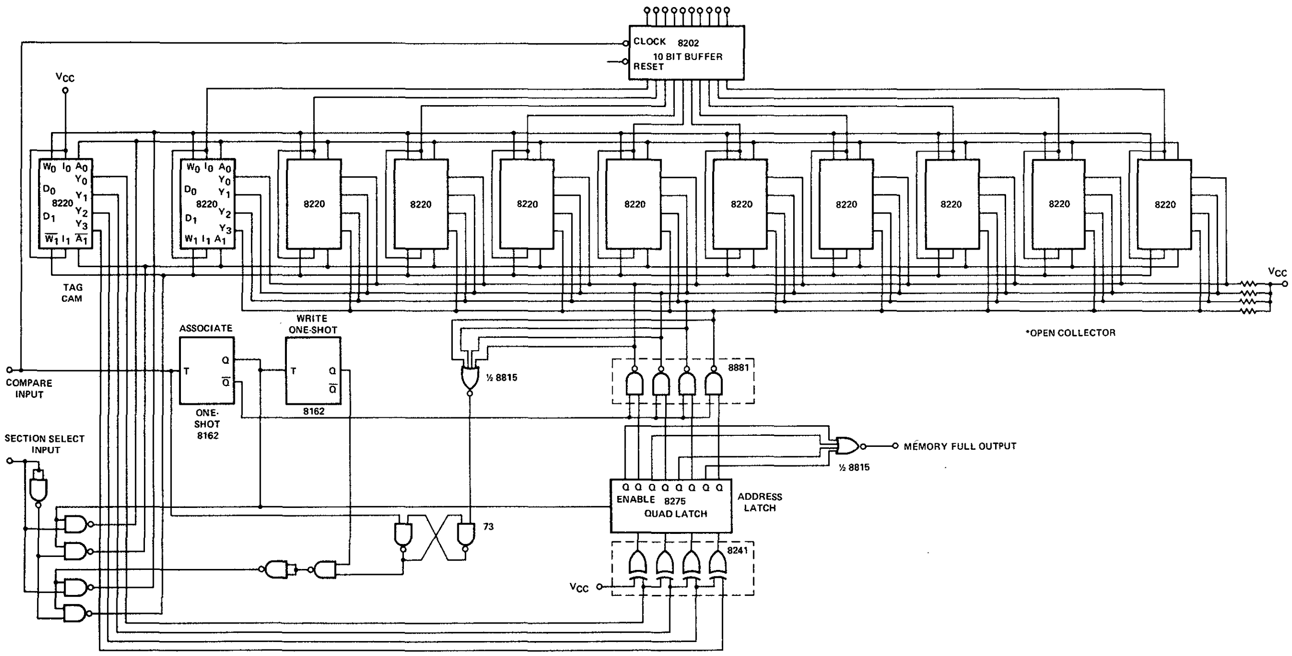
This system is a CAM array with peripheral IC circuitry designed to operate as a learning memory. It is organized in two sections of equal capacity, the total memory size (both sections) being 8 ten bit words. Either section can be selected through the section SELECT line, and the memory is easily expandable in the number of words and in word length.

By activating the COMPARE line, a new word is loaded into the buffer and is presented to the memory. Through the novel feature of data association, which is unique with CAM elements, the buffer's content is compared with the words stored in memory. If the input word, with which the memory was presented, is already contained in storage, no need for "learning" i.e. data acquisition, exists. This fact is indicated by a match from one of the Y_n lines ($Y_i = 1$) and thus no write command is initiated.

Before a WRITE operation is initiated, a location select has to be made such that the word to be written into the memory will go to the proper place. For this reason, a tag CAM is employed to keep track of memory locations, both empty and full. When a word is written into memory, a "1" is simultaneously written into the tag CAM. Thus, it is possible to keep track of the filled memory locations.

By monitoring the Y_n lines of the tag CAM, a convenient way of decoding an available address exists. Here exclusive OR circuitry is used which ensures that memory locations are filled successively when the need for "learning" exists. The quad latch is enabled before the write command is available to the CAM array. Thus the Y lines of unavailable memory locations are forced low ($Y_k = 0$).

APPLICATION: LEARNING MEMORY



256 BIT-BIPOLAR FIELD-PROGRAMMABLE ROM (32x8 PROM)

8223

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8223 is a TTL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip enable input is high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which permits wired AND operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum. The 8223 may be programmed to any desired pattern by the user. (See fusing procedure.) This feature is ideal for prototype hardware and systems requiring propriety codes.

A Truth Table/Order Blank is included on page 199 for ordering custom patterns.

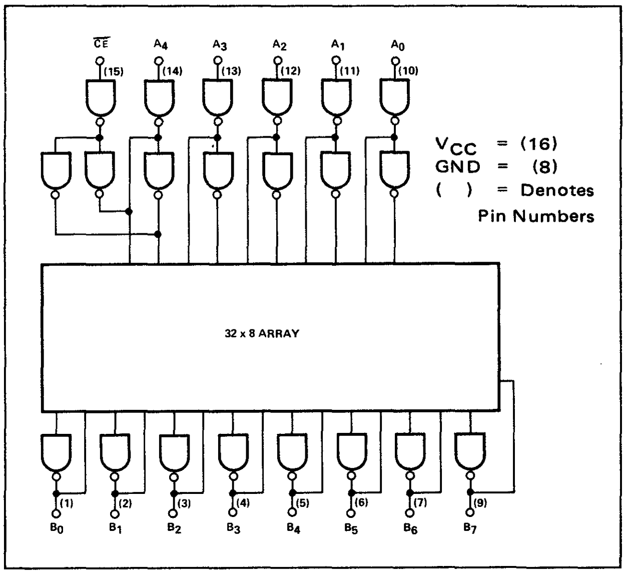
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- CHIP ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE FUSING PINS
- BOARD LEVEL PROGRAMMABLE

APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
"1" Output Leakage Current (N8223-)			100	μA			2.0V		13
(S8223-)			250	μA					
"0" Output Voltage (N8223-) (S8223-)			0.4	V	0.8V	2.0V	0.8V	9.6mA	6,10
(N8223-)			0.5	V	0.8V	2.0V	0.8V	16mA	6,10
"1" Input Current									
An, Address			40	μA		4.5V			
$\overline{\text{Chip Enable}}$ Input			80	μA			4.5V		
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1		-1.6	mA	0.4V		0.4V		

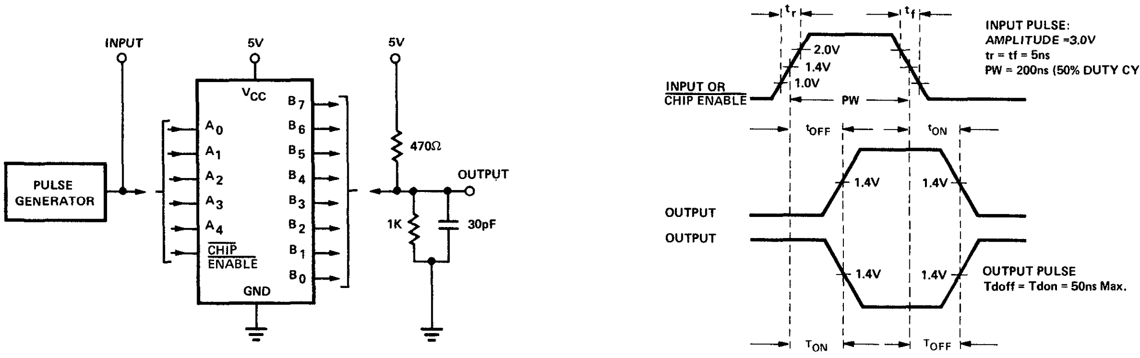
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP}}$ ENABLE	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
Propagation Delay									
An to Bn		35	50	ns				DC F.O.=12	7,12
$\overline{\text{Chip Enable}}$ to B_n		35	50	ns		4.5V		DC F.O.=12	7,12
Power Consumption		310/62	400/77	mW/mA		4.5V	4.5V		14
Input Latch Voltage	5.5			V			10mA		11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1" "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
14. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



Ground Pin 15 When Testing Address-Output Delays

8223 PROGRAMMING PROCEDURE

The 8223 may be programmed by using Curtis Electro Devices PR 23 Series or Spectrum Dynamics 300, 400 or 500 Series Programmers. Each performs the procedure outlined.

The 8223 Standard part is shipped with all outputs at logical "0". To write a logical "I" proceed as follows:

Programming Procedure A

Simple Programming Procedure using "bench" Equipment

1. Start with pin 8 grounded and V_{CC} removed from pin 16.
2. Remove any load from the outputs.
3. Ground the Chip Enable.
4. Address the desired location by applying ground (i.e., 0.4V maximum) for a "0", and +5.0V (i.e., +2.8V minimum) for a "1" at the address input lines.
5. Apply +12.5V to the output to be programmed through a 390 ohm ±10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for up to 1.0 second. If 1.0 second is exceeded, the duty cycle should be limited to a maximum of 25%. The V_{CC} overshoot should be limited to 1.0V maximum. If necessary, a clamping circuit should be used. The V_{CC} current requirement is 400 mA maximum at +12.5V. Several fuses can be programmed in sequence until 1.0 sec of high V_{CC} time is accumulated before imposing the duty cycle restriction.

   NOTE: Normal practice in test fixture layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A capacitor of 10 microfarads minimum, connected from the +12.5V to ground, should be located close to the unit being programmed.
7. Remove the programming voltage from pin 16.
8. Open the output.
9. Proceed to the next output and repeat, or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 8223.

Fast Programming Procedure — Programming Procedure B

1. Remove V_{CC} (open or ground pin 16).
2. Remove any load from the output.
3. Ground CE (pin 15).
4. Address the word to be programmed by applying 5 volts of a "1" and ground for a "0" to the address lines. (Solid TTL logic levels are ok, but we suggest buffer drivers or Utilogic OR/NOR gates for the addressing).
5. Apply 12.5V to the output to be programmed through 390 ohm ±10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for 25-50mS. Limit the V_{CC} overshoot to 1.0 volts max.
7. Reduce V_{CC} to ground (or open) and remove the load from the output.
8. Immediately repeat steps 5 and 6 for other outputs of the same word, or repeat 4 through 6 for a different word. Continue programming for a max of 1 second. Then remove power for 4 seconds and continue until the entire bit pattern is programmed.

After programming the 8223, the unit should be checked to insure the code is correct. If additional fuses must be opened, they may be programmed during verification.

Fast Programming Procedure — Programming Procedure C

Steps 1 through 5 are the same as in Procedure B.

6. Apply a 5mS pulse to V_{CC} (pin 16). Limit the V_{CC} overshoot.
7. Reduce V_{CC} to 5 volts for 10-15uS and verify the fuse opened (output is now a "1". If the bit programmed go on to the next bit to be programmed. If the bit did not program, then reduce V_{CC} to ground (or open) for 1-5uS and repeat step 6 and 7 until the fuse programs (1 second total time max).
8. Continue programming at this rate for 1 second. Remove all power from the device for 4 seconds then continue programming procedure.

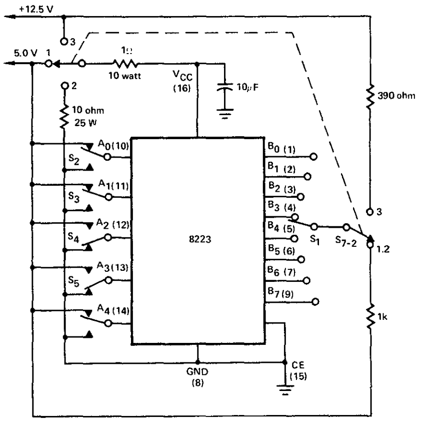
V_{CC} Waveform

BOARD LEVEL PROGRAMMING PROCEDURE FOR THE 8223

The chip select controls which 8223 is being programmed when several PROMS are collector OR'd. To program in this manner, the only changes required are:

1. The 390 ohm resistor is reduced to $\frac{200}{N}$ ohm where N is the number of outputs tied together ($2 \leqslant N \leqslant 12$).
2. Reduce max fuse pulse width from 1 second max to 0.92 sec max.

MANUAL PROGRAMMER DIAGRAM



S_1 = Single pole 9 position switch

S_2 through S_6 = single pole 2 position switch

S_7 = Two pole 3 position switch with ground connected to the middle position of the section connected to V_{CC}, pin 16 to go from 5 volts to 12.5V the switch will momentarily ground V_{CC}) and positions 1 and 2 of the other section connected to 5.0V to provide the needed 5 volts to the output for verification.

NOTE: 1. The 10μf capacitor across pin 16 to ground is required to eliminate noise from V_{CC}.

256-BIT BIPOLAR ROM (32x8 ROM) 8224

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8224 is a TTL 256 Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Enable input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Enable input is taken high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-AND operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum.

The 8224–CB180 has been programmed to convert the seven bit ASC II alphabet code to the 8 bit EBCDIC Alphabet code. The conversion includes the letters A through Z. With the addition of gating circuitry, the 8224–CB180 will convert both upper case and lower case letters.

Customer specified patterns are also available as custom products. **Refer to page 250 for Truth Table/Order Blank.**

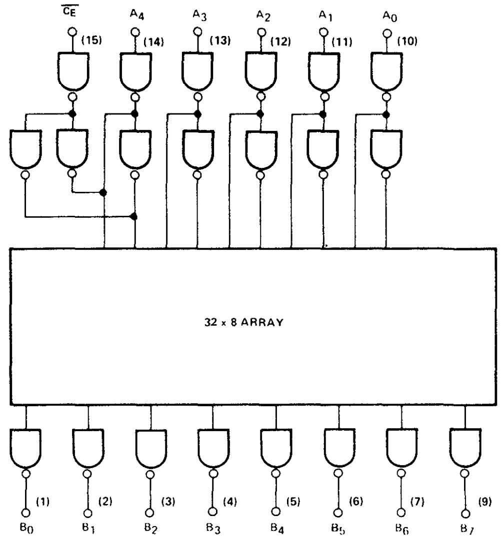
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- CHIP ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATOR
CONTROL STORE

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS			TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	MAX.	UNITS	V_{CC}	A_n "0"	A_n "1"	$\overline{\text{CHIP ENABLE}}$		
"1" Output Leakage Current		100	µA	5.00			2.0V		13
"0" Output Voltage		0.4	V	4.75	0.8V	2.0V	0.8V	9.6mA	6,10
		0.4	V	5.00	0.8V	2.0V	0.8V	9.6mA	6,10
		0.4	V	4.75	0.8V	2.0V	0.8V	9.6mA	6,10
"1" Input Current									
An, Address		40	µA	5.25		4.5V	4.5V		
$\overline{\text{Chip Enable}}$ Input		80	µA	5.25			4.5V		
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1	-1.6	mA	5.25	0.4V		0.4V		

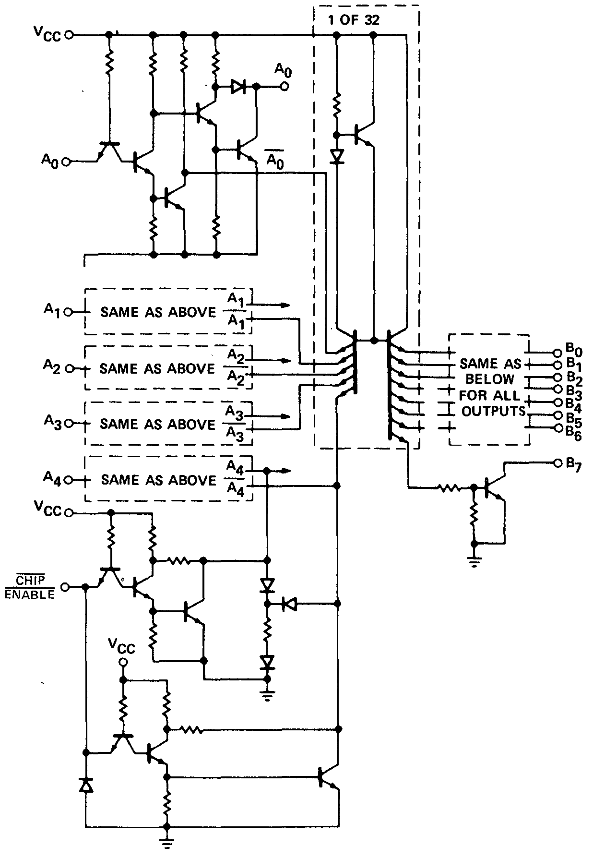
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS			TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	MAX.	UNITS	V_{CC}	A_n "0"	A_n "1"	$\overline{\text{CHIP ENABLE}}$		
Propagation Delay									
An to Bn		50	ns	5.00				DC F.O.=12	7,12
$\overline{\text{Chip Enable}}$ to Bn		50	ns	5.00		4.5V		DC F.O.=12	7,12
Power Consumption		400	mW	5.25		4.5V	4.5V		
Input Latch Voltage	5.5		V	5.00	10mA		10mA		11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.

SCHEMATIC DIAGRAM



CODE CONVERSION ASCII TO EBCDIC (UPPER & LOWER CASE LETTERS ONLY) 8224-CB180

ASC II CODE							CHARACTER	EBCDIC CODE
B_7	B_6	B_5	B_4	B_3	B_2	B_1		0 1 2 3 4 5 6 7
0	0	0	X	X	X	X	--	Not Decoded
0	0	1	X	X	X	X	--	Not Decoded
0	1	0	X	X	X	X	--	Not Decoded
0	1	1	X	X	X	X	--	Not Decoded
1	0	0	0	0	0	0	--	Not Decoded
1	0	0	0	0	0	1	A	1 1 0 0 0 0 0 1
1	0	0	0	0	1	0	B	1 1 0 0 0 0 1 0
1	0	0	0	0	1	1	C	1 1 0 0 0 0 1 1
1	0	0	0	1	0	0	D	1 1 0 0 0 1 0 0
1	0	0	0	1	0	1	E	1 1 0 0 0 1 0 1
1	0	0	0	1	1	0	F	1 1 0 0 0 1 1 0
1	0	0	0	1	1	1	G	1 1 0 0 0 1 1 1
1	0	0	1	0	0	0	H	1 1 0 0 1 0 0 0
1	0	0	1	0	0	1	I	1 1 0 0 1 0 0 1
1	0	0	1	0	1	0	J	1 1 0 1 0 0 0 1
1	0	0	1	0	1	1	K	1 1 0 1 0 0 1 0
1	0	0	1	1	0	0	L	1 1 0 1 0 0 1 1
1	0	0	1	1	0	1	M	1 1 0 1 0 1 0 0
1	0	0	1	1	1	0	N	1 1 0 1 0 1 0 1
1	0	0	1	1	1	1	O	1 1 0 1 0 1 1 0
1	0	1	0	0	0	0	P	1 1 0 1 0 1 1 1
1	0	1	0	0	0	1	Q	1 1 0 1 1 0 0 0
1	0	1	0	0	1	0	R	1 1 0 1 1 0 0 1
1	0	1	0	0	1	1	S	1 1 1 0 0 0 1 0
1	0	1	0	1	0	0	T	1 1 1 0 0 0 1 1
1	0	1	0	1	0	1	U	1 1 1 0 0 1 0 0
1	0	1	0	1	1	0	V	1 1 1 0 0 1 0 1
1	0	1	0	1	1	1	W	1 1 1 0 0 1 1 0
1	0	1	1	0	0	0	X	1 1 1 0 0 1 1 1
1	0	1	1	0	0	1	Y	1 1 1 0 1 0 0 0
1	0	1	1	0	1	0	Z	1 1 1 0 1 0 0 1
1	0	1	1	0	1	1	--	1 Not Decoded
1	0	1	1	1	0	0	--	1 Not Decoded
1	0	1	1	1	0	1	--	1 Not Decoded
1	0	1	1	1	1	0	--	1 Not Decoded
1	0	1	1	1	1	1	--	1 Not Decoded
1	1	0	0	0	0	0	--	1 Not Decoded
1	1	0	0	0	0	1	a	1 0 0 0 0 0 0 1
1	1	0	0	0	1	0	b	1 0 0 0 0 0 1 0
1	1	0	0	0	1	1	c	1 0 0 0 0 0 1 1
1	1	0	0	1	0	0	d	1 0 0 0 0 1 0 0
1	1	0	0	1	0	1	e	1 0 0 0 0 1 0 1
1	1	0	0	1	1	0	f	1 0 0 0 0 1 1 0
1	1	0	0	1	1	1	g	1 0 0 0 0 1 1 1
1	1	0	1	0	0	0	h	1 0 0 0 1 0 0 0
1	1	0	1	0	0	1	i	1 0 0 0 1 0 0 1
1	1	0	1	0	1	0	j	1 0 0 1 0 0 0 1
1	1	0	1	0	1	1	k	1 0 0 1 0 0 1 0
1	1	0	1	1	0	0	l	1 0 0 1 0 0 1 1
1	1	0	1	1	0	1	m	1 0 0 1 0 1 0 0
1	1	0	1	1	1	0	n	1 0 0 1 0 1 0 1
1	1	0	1	1	1	1	o	1 0 0 1 0 1 1 0
1	1	1	0	0	0	0	p	1 0 0 1 0 1 1 1
1	1	1	0	0	0	1	q	1 0 0 1 1 0 0 0
1	1	1	0	0	1	0	r	1 0 0 1 1 0 0 1
1	1	1	0	0	1	1	s	1 0 1 0 0 0 1 0
1	1	1	0	1	0	0	t	1 0 1 0 0 0 1 1
1	1	1	0	1	0	1	u	1 0 1 0 0 1 0 0
1	1	1	0	1	1	0	v	1 0 1 0 0 1 0 1
1	1	1	0	1	1	1	w	1 0 1 0 0 1 1 0
1	1	1	1	0	0	0	x	1 0 1 0 0 1 1 1
1	1	1	1	0	0	1	y	1 0 1 0 1 0 0 0
1	1	1	1	0	1	0	z	1 0 1 0 1 0 0 1
1	1	1	1	0	1	1	--	Not Decoded
1	1	1	1	1	0	0	--	Not Decoded
1	1	1	1	1	0	1	--	Not Decoded
1	1	1	1	1	1	0	--	Not Decoded
1	1	1	1	1	1	1	--	Not Decoded

TRUTH TABLES FOR 8224-CB180

INPUT PINS						OUTPUT PINS							
15	14	13	12	11	10	9	7	6	5	4	3	2	1
$\overline{CE}$	A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	1	1	0	1	0	0	0	1	1
0	0	0	1	1	0	0	1	1	0	0	0	1	1
0	0	0	1	1	1	1	1	1	0	0	0	1	1
0	0	1	0	0	0	0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1	0	0	1	1
0	0	1	0	1	0	1	0	0	0	1	0	1	1
0	0	1	0	1	1	0	1	0	0	1	0	1	1
0	0	1	1	0	0	1	1	0	0	1	0	1	1
0	0	1	1	0	1	0	0	1	0	1	0	1	1
0	0	1	1	1	0	1	0	1	0	1	0	1	1
0	1	0	0	0	0	1	1	1	0	1	0	1	1
0	1	0	0	0	1	0	0	0	1	1	0	1	1
0	1	0	0	1	0	1	0	0	1	1	0	1	1
0	1	0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	1	0	0	1	1	0	0	0	1	1	1
0	1	0	1	0	1	0	0	1	0	0	1	1	1
0	1	0	1	1	0	1	0	1	0	0	1	1	1
0	1	0	1	1	1	0	1	1	0	0	1	1	1
0	1	1	0	0	0	1	1	1	0	0	1	1	1
0	1	1	0	0	1	0	0	0	1	0	1	1	1
0	1	1	0	1	0	1	0	0	1	0	1	1	1
0	1	1	0	1	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	1	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0	0	0	0	0
1	x	x	x	x	x	1	1	1	1	1	1	1	1

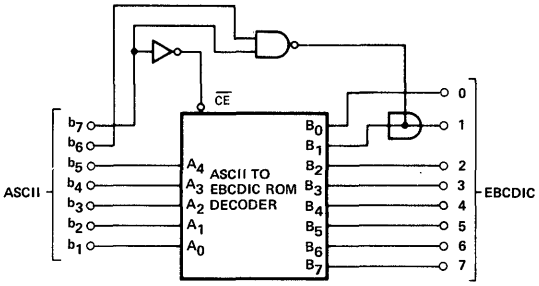
TYPICAL APPLICATIONS

To select the ROM only when addressed by an upper or lower case alphabet character, the following truth table applies:

	Upper Case		Lower Case	
ASCII	0	0	1	1
ASCII	0	1	0	1
$\overline{\text{CHIP ENABLE}} = \overline{B_7}$	1	1	0	0
EBCDIC #1 OUTPUT = $\overline{B_6 \cdot B_7}$	1	1	1	0

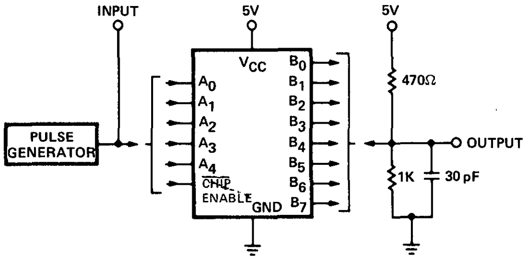
Thus, the ASCII to EBCDIC ROM standard product plus gating as shown performs the complete conversion.

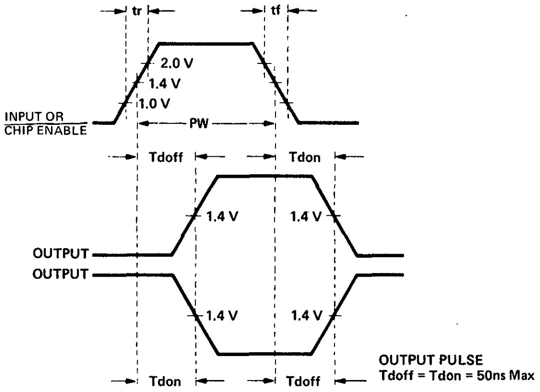
TYPICAL APPLICATIONS (Cont'd)



GROUND PIN 15 WHEN TESTING ADDRESS-OUTPUT DELAYS

AC TEST FIGURE AND WAVEFORMS





INPUT PULSE:
Amplitude = 3.0V
tr = tf = 5ns
PW = 200ns (50% DUTY CYCLE)

64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM) 8225

THIS PRODUCT AVAILABLE IN 0°C TO 75°C TEMP RANGE ONLY.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8225 is a TTL 64-bit Read-Write Random Access Memory organized as 16-words of 4 bits each. The 8225 is ideally suited for application in scratch pads and high-speed buffer memories.

Words are selected through a 4-input binary decoder when the chip enable input $(\overline{C}_E)$ is at logic "0". Data is written into the memory when Read Enable (R_E) is at logic "0" and read from the memory when RE is at logic "1".

The outputs of the 8225 are logical "1" during write operation, therefore, inputs and outputs can be commoned in busses to reduce the number of I/O leads. Output collectors are uncommitted.

FEATURES

- CHIP ENABLE LINE FOR EXPANSION
- OPEN COLLECTOR OUTPUTS FOR EXPANSION
- ON THE CHIP DECODING
- ALL OUTPUTS "1" DURING WRITING
- DIODE PROTECTED INPUTS

APPLICATIONS

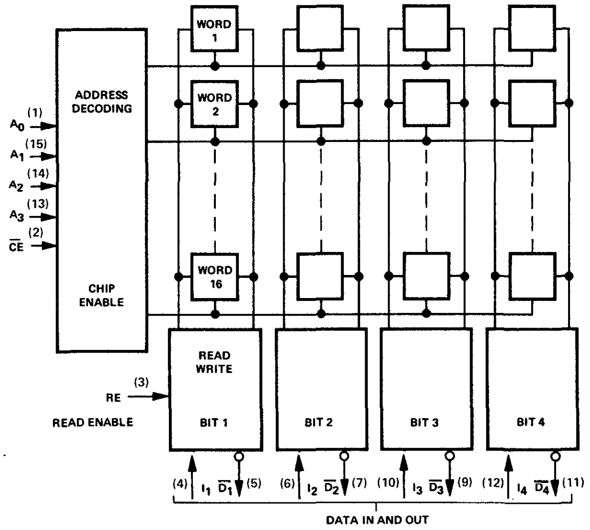
SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS (First in-first out)
CONTROL STORE

TRUTH TABLE

RE	$\overline{CE}$ (Chip Enable)	MODE	OUTPUTS
0	0	Write	"1"
1	0	Read	Information
X	1	Chip Disable	"1"

X = Either State

BLOCK DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

"ONE" LEVEL IN OR DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				CHIP ENABLE	INPUTS		DATA INPUTS	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS		WRITE	ADDRESS			
"0" Output Voltage			.4	V	.8V	Pulse			16mA	8, 11, 12
"1" Output Leakage Current			100	μA	.8V	Pulse		.8V	5.25V	11, 12
"0" Input Current	-.1		-1.6	mA	.4V	.4V	.4V	.4V		16
"1" Input Current										
Chip Enable			80	μA	4.5V					
Write, Address, Data			40	μA	4.5V	4.5V	4.5V	4.5V		16

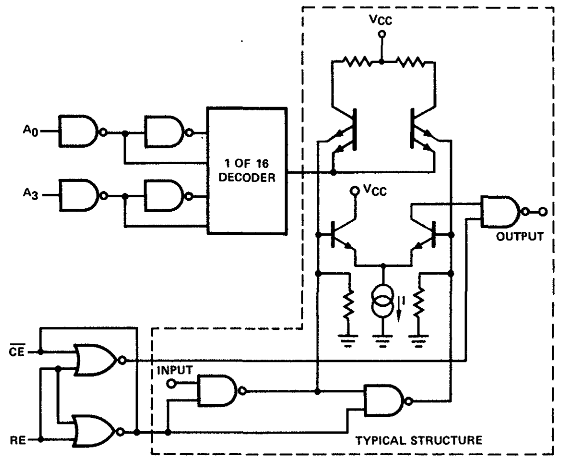
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				CHIP ENABLE	INPUTS		DATA INPUTS	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS		WRITE	ADDRESS			
Minimum Write Pulse Width (W_{PW})		18	30	ns						
Input Setup Time (I_{SU})		18	20	ns						
Input Hold Time (I_{HO})		0	5	ns						
Address Setup Time (A_{SU})			5	ns						
Address Hold Time (A_{HO})			5	ns						
Access Time (T_A)	20	35	50	ns						17
Read Recovery Time (T_{RR})	20	35	50	ns						17
Data Pulse Width (D_{PW})	20			ns						
Write Recovery Time (T_{WR})		25	40	ns						
Write Access Time (T_{WA})		25	40	ns						
Chip Enable Recovery Time (T_{CR})		20	30	ns						
Chip Enable Access Time (T_{CA})		20	30	ns						
Input Clamp Voltage			-1.5	V	-12mA	-12mA	-12mA	-12mA		16
Input Latch Voltage - except Data			5.5	V	10mA	10mA	10mA			16
Data			5.5	V	5V	5V		10mA		16
Power Consumption		400	552	mW	0V	5V	0V	0V		14

NOTES:

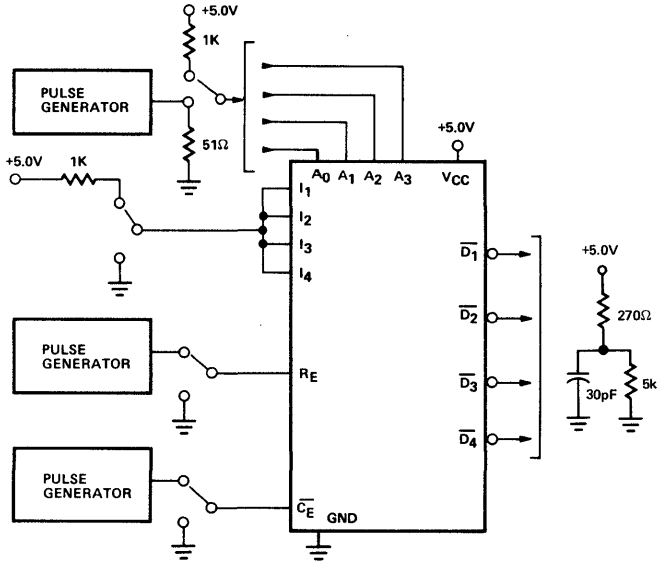
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Capacitance is measured on Boonton Electronic Corporation Model 75A-53 Capacitance Bridge or equivalent. f = 1 MHz, $V_{ac} = 25m\ V_{rms}$.
7. All pins not specifically referenced are tied to ground for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{CC}.
9. One DC fan-out is defined as 0.8mA.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
12. For any given binary code on the Address Inputs the Write input must be momentarily brought to a logical "0" level.
13. See AC test circuits on following pages.
14. All sense outputs in "0" state.
15. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
16. Test each input one at a time.
17. Address Pulse Width (A_{PW}) is 40ns for this test.

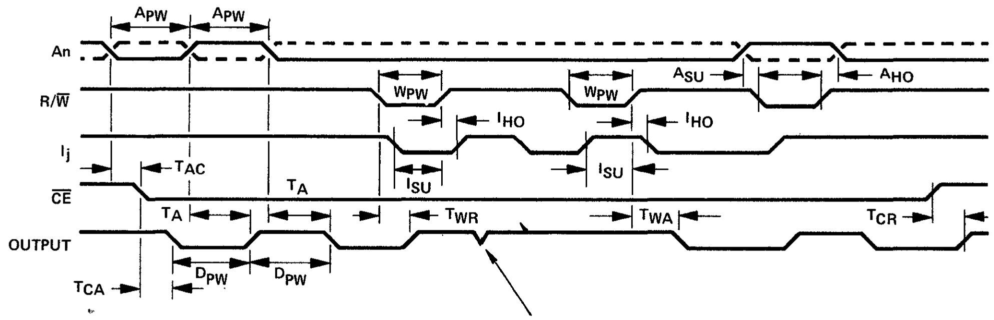
FUNCTIONAL DIAGRAM



ONE LEVEL IN ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

AC TEST FIGURES AND WAVEFORMS





NOTE: NEGATIVE TRANSISTIVE
DOES NOT GO BELOW 2.6
VOLTS AND GENERALLY
IS NOT MEASURABLE.

4096 BIT BIPOLAR ROM
(1024x4 ROM)

8228

THIS PRODUCT AVAILABLE IN 0°C TO 75°C TEMPERATURE RANGE ONLY

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8228 is a 4096 Bit Bipolar Read Only Memory organized as 1024 words by 4 bits per word. Available in a 16 pin dual in-line package, the 8228 can provide very high bit packing density by replacing four standard 256X4 ROMS.

The 8228 is fully TTL compatible and includes on-the-chip decoding. Typical access time is 50ns with a power consumption of only .125mW per bit.

The standard 8228 ROM pattern is the USASCII Row Character Generator code; however, custom patterns are also available. The standard pattern is specified as the N8228I - CD162, while custom circuits are identified as N8228I - CXXX. A truth table/order blank is included on page 254 for ordering custom patterns.

See page 242 for CD162 Pattern and USASCII Row Character Generator.

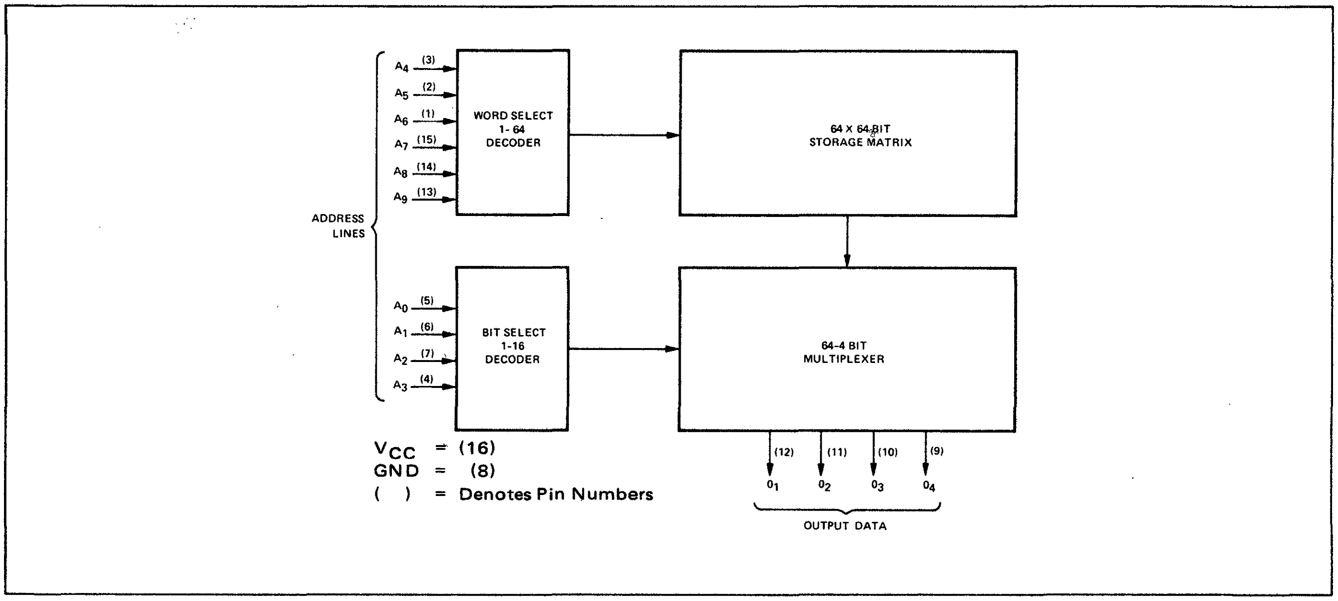
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TOTEM POLE OUTPUTS
- DIODE PROTECTED INPUTS
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)

APPLICATIONS

MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATION
CONTROL STORE

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	LIMITS UNITS	TEST CONDITIONS	NOTES
"0" Output Voltage			0.5	V	I_{out} = 11.2 mA	
"1" Output Voltage	2.7			V	I_{out} = -1.0 mA	
"0" Input Current		-10	-200	µA	V_{in} = 0.5V	
"1" Input Current		1	25	µA	V_{in} = 5.25V	
Input Threshold Voltage						
"0" Level	.85			V		
"1" Level			2.0	V		
Propagation Delay		50	90	ns		

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Input Clamp Voltage	–1.0			V	I_{in} = 5.0mA	
Power Consumption		100	140	mA	0_1 to 0_3 = "0"	
Output Short Circuit Current	–20		–70	mA		

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{CC} = 5.0V)

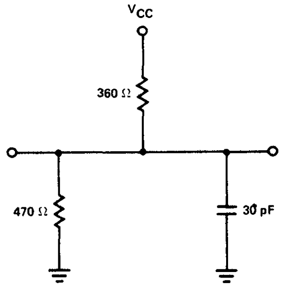
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Access Time–Address to Output		50	75	ns		5

NOTES:

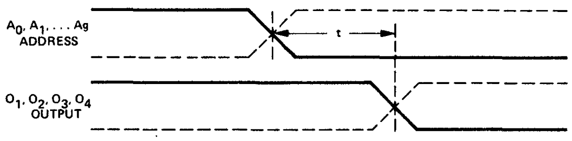
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 5.5V
   Input currents must not exceed ±30mA
   Output currents must not exceed ±100mA
   Storage temperature must be between -60°C to +150°C
5. Rise and fall time for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

AC TEST FIGURE AND WAVEFORM

TEST LOAD



READ CYCLE



256 BIT BIPOLAR RAM (256x1 RAM)
(82S06 TRI-STATE) (82S07 OPEN COLLECTOR)

82S06
82S07

THESE PRODUCTS ARE AVAILABLE IN 0°C to 70°C TEMPERATURE RANGE ONLY
OBJECTIVE SPECIFICATION

AVAILABLE SOON

DIGITAL INTEGRATED CIRCUITS

DESCRIPTION

The 82S06 and 82S07 are ideal devices for use in Control Stores, small buffers, scratch pads, "cache" type buffer stores, memory maps, etc. The typical read time (the time between applying an address and obtaining valid output data) is 30ns. The typical write time (the time between applying one address and storing data) is 30ns. The circuit has 3 chip enable inputs which greatly simplifies the circuit configuration when used in large memories. The 82S06 and 82S07 also feature very low input loadings, 25 microamperes for a "1" state and -100 microamperes for "0".

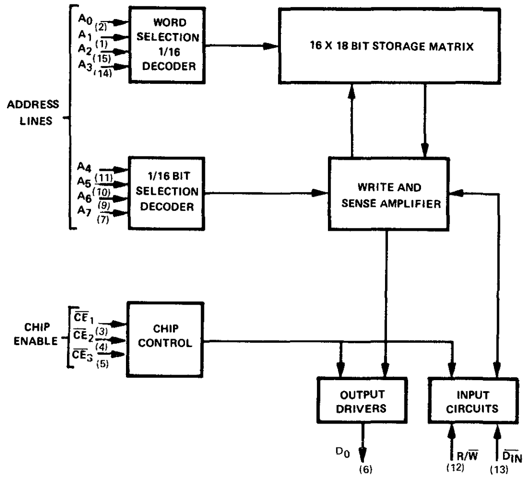
The memories are TTL compatible and operate from single 5 volt supply.

FEATURES

- **256 X 1 ORGANIZATION**
- **30 NANOSECOND ACCESS TIME TYPICAL**
- **LOW 1.5 mw/BIT POWER DISSIPATION TYPICAL**
- **LOW 100 µA INPUT LOADING**
- **TRI-STATE (82S06) OR OPEN COLLECTOR (82S07) OUTPUT**
- **ON CHIP DECODING**

BLOCK DIAGRAM

256 BIT BIPOLAR RANDOM ACCESS MEMORY



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

"ONE" LEVEL IN ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 0 to 75°C, V_{CC} = 5.0V ±5) Note 1, 2, 3

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Input Current		−10	−100	µA	V_{in} = 0.5V	
"1" Input Current		<1.0	25	µA	V_{in} = 5.25V	
"0" Output Voltage		.25	.5	V	I_{out} = 16mA	
Output Leakage Current (82S07)		<1.0	100	µA	$\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ = "1", V_{out} = 2.7V	
Output "off" Current (82S06)		<1.0	±100	µA	$\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ = "1", $0.5 \leq V_{out} \leq 2.7V$	
"0" Input Threshold	.85			V		
"1" Input Threshold			2.0	V		
Power Supply Drain		75	100	mA	V_{CC} = 5.00V	
Input Clamp Voltage	−1.0	−.5		V	I_{in} = −5.0mA	
Input Capacitance		5		pF		
Output Capacitance		8		pF		

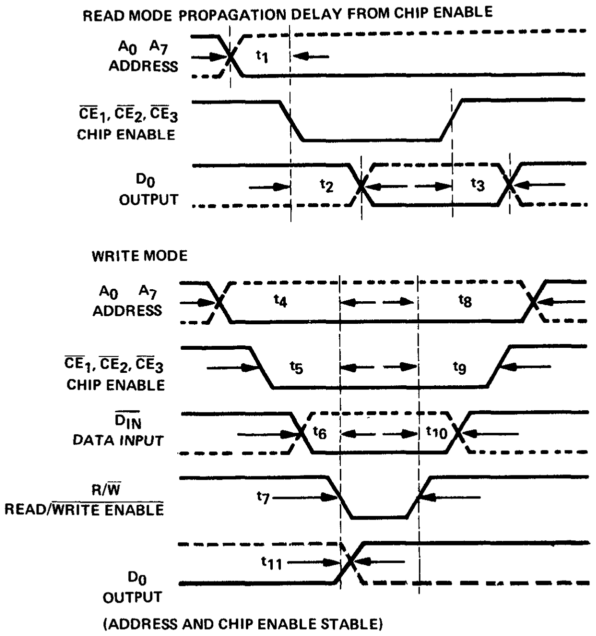
OBJECTIVE ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0V$)

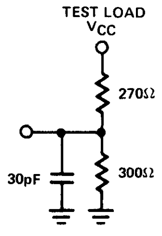
CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN.	TYP.	MAX.	UNITS		
Access Time—Address to Output			30		ns		4
Address Set-Up Time (read)	t_1		10		ns		
Propagation Delay			20		ns		4
Chip Enable to Output Enable	t_2		20		ns		
Propagation Delay			15		ns		4
Chip Enable to Output Disable	t_3		15		ns		
Address to Write Enable			5		ns		4
Set-Up Time	t_4		5		ns		
Chip Enable to Write Enable			0				4
Set-Up Time	t_5		0		ns		
Data Input to Write Enable			0				4
Set-Up Time	t_6		0		ns		
Write Enable Plus Width	t_7		15		ns		4
Address Hold Time	t_8		0		ns		4
Chip Enable Hold Time	t_9		0		ns		4
Data Input Hold Time	t_{10}		0		ns		4
Write Enable Propagation Delay	t_{11}		30		ns		4
Output Short Circuit Current (82S06)		−20		−100	mA	$V_{out} = 0V$	4

NOTES:

1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltages must not exceed 6.0V, Input currents must not exceed ±30mA, Output currents must not exceed ±100mA, Storage temperature must be between -60°C to +150°C.
4. Refer to Timing Diagram for definition of terms and test load.

TIMING DIAGRAM





MEMORY TIMING DESCRIPTION

t_1 = set up time for an address input to chip enable for valid data at output
t_2 = propagation delay from chip enable to valid data at output
t_3 = propagation delay from chip disable to output turn off
t_4 = set up time from address to write enable
t_5 = set up time from chip enable to write enable
t_6 = set up time from data input to write enable
t_7 = write enable pulse width
t_8 = hold time for address from write enable
t_9 = hold time for chip enable from write enable
t_{10} = hold time for data input from write enable
t_{11} = propagation delay from write enable to valid data at output

NOTE:
Rise and fall times for test must be less than 5 ns between 10-90% points, $V_{CC} = 5.0V$, input amplitudes 2.8V, all measurements made at 1.5V level. Times are given in nanoseconds.

HIGH SPEED WRITE-WHILE-READ
64-BIT BIPOLAR RAM (32x2 RAM)

82S21

THIS PRODUCT AVAILABLE IN 0°C TO 75°C TEMPERATURE RANGE ONLY

AVAILABLE SOON

OBJECTIVE SPECIFICATION

DESCRIPTION

The 82S21 is a TTL 64 bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1". $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

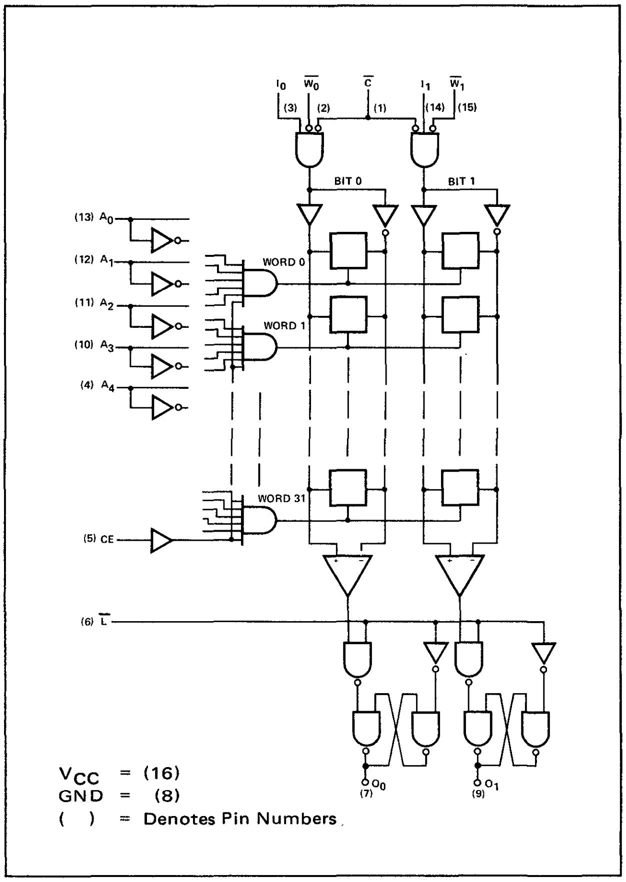
FEATURES

- BUFFERED ADDRESS LINES
- ON CHIP LATCHES
- ON CHIP DECODING
- BIT MASKING CONTROL LINES
- ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS WITH 48 mA CAPABILITY
- PROTECTED INPUTS
- VERY HIGH SPEEDS (25ns TYP)

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

LOGIC DIAGRAM



TRUTH TABLE

CE	$\overline{C}$	$\overline{W_0}$	$\overline{W_1}$	$\overline{L}$	Mode	Outputs
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	1	0	X	Write Data into Bit 0 Only	If $\overline{L}$ = 0: Data from last word address when L went from "1" to "0"
1	0	0	1	X	Write Data into Bit 1 Only	If $\overline{L}$ = 1: Data being written into the selected bit location and stored in other addressed location

OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{CC} = 5.0V)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			.5	V	V_{out} = 40mA	
"1" Output Leakage Current			250	μA	V_{out} = 5.5V	
"0" Input Current (All Inputs)			–1.6	mA	V_{in} = 0.5V	
"1" Input Current (All Inputs			40	μA	V_{in} = 2.4V	
Input "0" Threshold Voltage			0.85	V		
Input "1" Threshold Voltage	2.0			V		
Power Supply Current			150	mA		
Read Access Time Address to Output t_1		25		ns		
Address Set-Up Time Address to Latest C(–) or W(–) t_2		8		ns		5
Data Set-Up Time to Latest C(–) or W(–) t_3		8		ns		5
Address Hold Time Earliest C(+) or W(+) to Address t_4		0		ns		5
Control or Write Pulse Width t_5		20		ns		
Write Access Time Latest I_x or W(–) or C(–) to Output t_6		25		ns		5
Latch Output Set-Up Time Output to L(–) t_7		0		ns		5
Latch Address Hold Time L(–) to Address t_8		10		ns		5
Delatch Access Time L(+) to Output t_9		15		ns		5
Data Hold Time Earliest C(+) or W(+) to I_x t_{10}		5		ns		5

NOTES:

1. Positive current is defined as into the Terminal.
2. No more than one output should be grounded at the same time.
3. Applied voltages must not exceed 5.5V.
   Input current must not exceed ±12 mA.
   Output current must not exceed ±100 mA.
   Storage temperature must be within the –60°C to +150°C range.
4. Manufacturer reserves the right to make design and process changes and improvements.
5. (+) means positive going transition of the voltage signal.
   (–) means negative going transition of the voltage signal.

AC WAVEFORMS

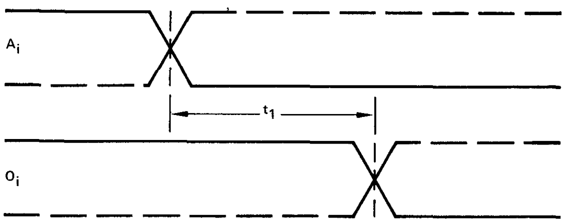


Fig. 1 Read Access Time

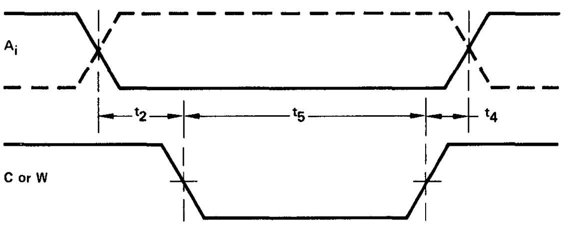


Fig. 2 Address Setup and Hold Time

AC WAVEFORMS

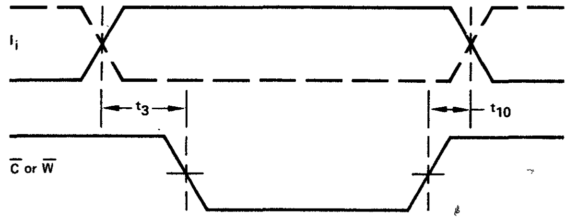


Fig. 3 Data Setup and Hold Time

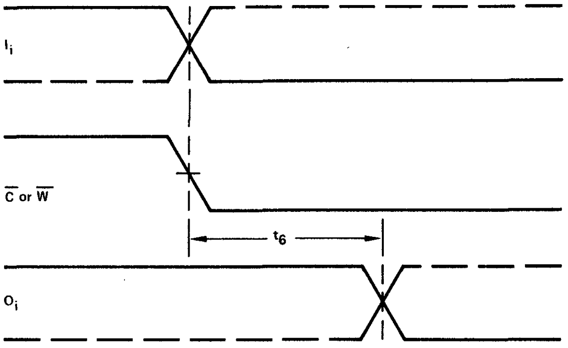


Fig. 4 Write Access Time

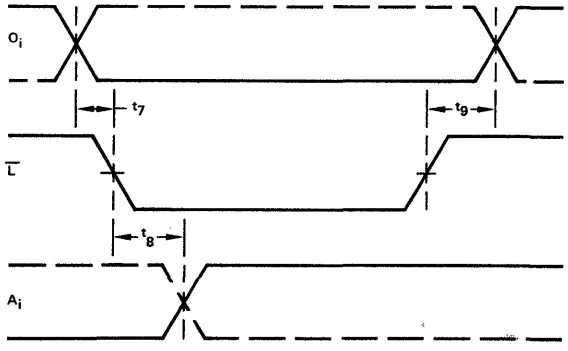
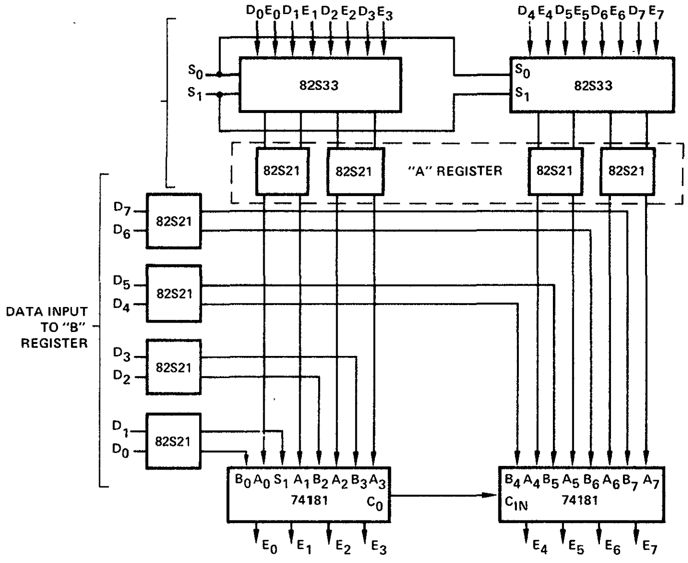


Fig. 5 Latch Times

TYPICAL APPLICATION



BASIC 8 BIT FULLY BUFFERED ACCUMULATOR

By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32 x 8 RAM register. Data is loaded directly into the "B" register. With this arrangement, *the function A+B —— A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.*

1024 BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM) (82S26 OPEN COLLECTOR) (82S29 TRI-STATE)

82S26 82S29

AVAILABLE IN 0°C TO 75°C TEMPERATURE RANGE ONLY

AVAILABLE SOON

OBJECTIVE SPECIFICATION

DESCRIPTION

The 82S26 (open Collector Outputs) and the 82S29 (tri State Outputs) are Bipolar 1024 Bit Read Only Memories organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. Two chip enable lines are provided and the outputs are bussable to allow for memory expansion capability.

The 82S26 and 82S29 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35ns.

The standard 82S26 and 82S29 are supplied with all outputs at a logical "0". If a programmed unit is required the Truth Table/Order Blank on page 252/253 can be used.

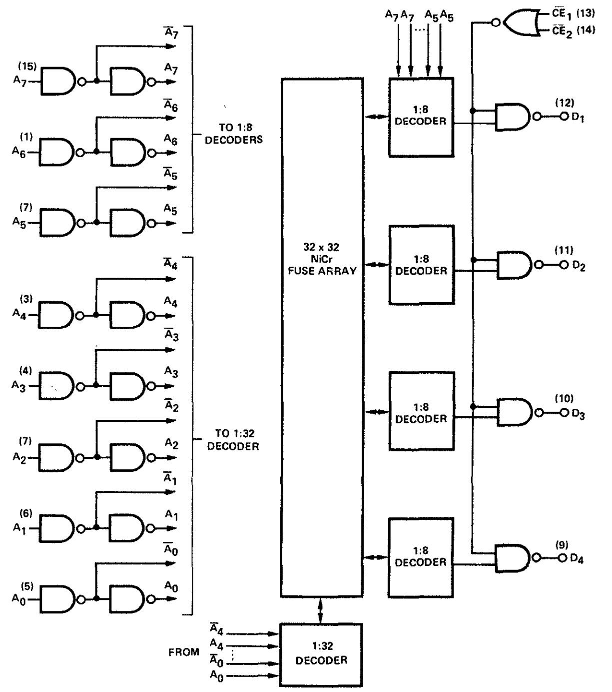
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TWO CHIP ENABLE LINES
- OPEN COLLECTOR OR TRI STATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- BOARD LEVEL PROGRAMMABLE

APPLICATIONS

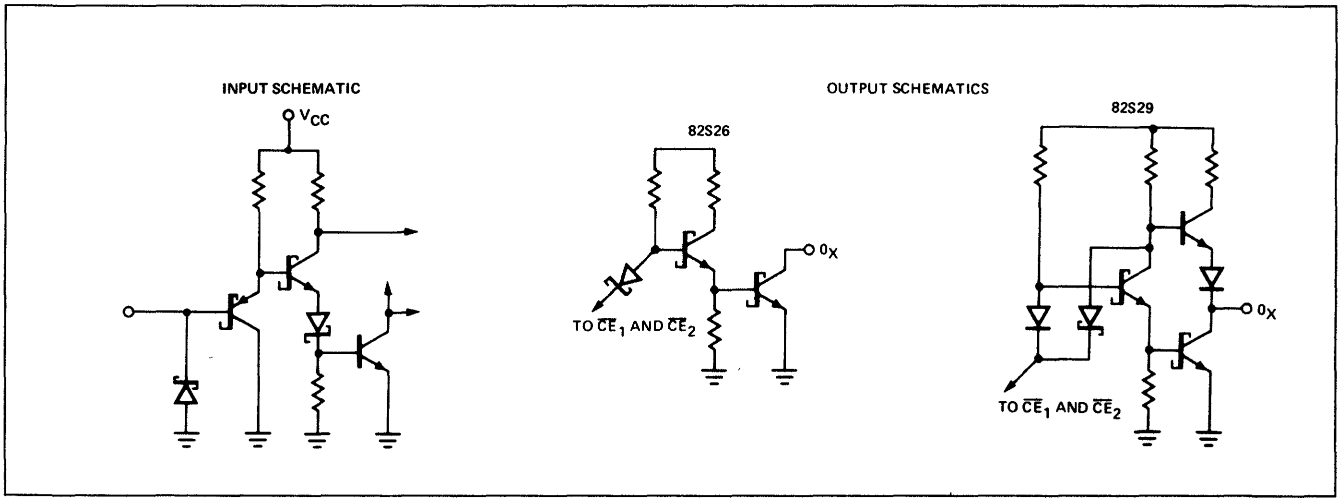
PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CONTROL STORE

BLOCK DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

INPUT/OUTPUT SCHEMATIC DIAGRAMS



OBJECTIVE ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
"0" Output Voltage			0.5	V	I_{out} = 16mA
"1" Output Leakage (82S26)			40	μA	$\overline{CE_1}$ or $\overline{CE_2}$ = "1", V_{out} = 2.6V
(82S29)			100	μA	$\overline{CE_1}$ = $\overline{CE_2}$ = "0", V_{out} = 2.6V
(82S29)	–40		+40	μA	$\overline{CE_1}$ or $\overline{CE_2}$ = "1", V_{out} = 0.5 to 2.4V
"1" Output Current (82S29)	–2.0			mA	$\overline{CE_1}$ = $\overline{CE_2}$ = "0", V_{out} = 2.4V
"0" Input Current			–250	μA	V_{in} = 0.5V
"1" Input Current			50	μA	V_{in} = 2.7V
Input Threshold Voltage					
"0" Level	.85			V	
"1" Level			2.0	V	

(T_A = 25°C and V_{CC} = 5.0V)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Input Clamp Voltage	–1.0			V	I_{in} = 5.0mA
Power Consumption		105/525		mA/mW	V_{CC} = 5.00V
Propagation Delay					
Address to Output			60	ns	
$\overline{\text{Chip Enable}}$ to Output			50	ns	

1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltage must not exceed 6.0V except while programming.
   Input currents must not exceed ±30 mA.
   Output currents must not exceed ±50mA except while programming.
4. Specifications are tentative. Final specifications will be available by May 1972.

PROGRAMMING PROCEDURE

The 82S26 and 82S29 may be programmed by using the Curtis Electro Devices or Spectrum Dynamics Programmers. Each perform the procedures outlined.

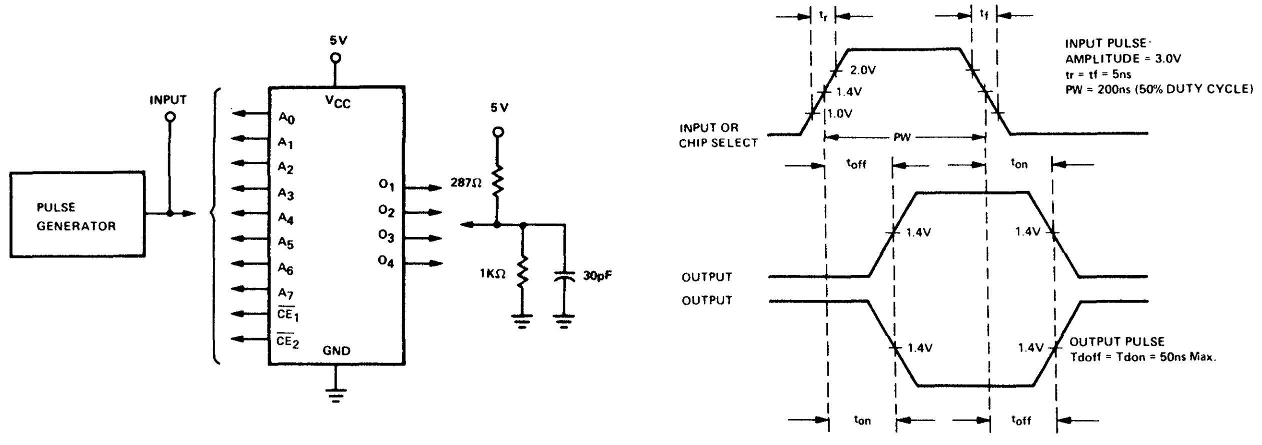
The 82S26 and 82S29 standard parts, are shipped with all outputs at Logical "0". To write a logical "1" proceed as follows:

A. Simple Programming Procedure using "bench" equipment.
   1. Connect pin 8 (Gnd) to ground. Enable the device by connecting $\overline{CE_1}$, (pin 13) and $\overline{CE_2}$ (pin 14) to a logical "0".
   2. Raise V_{CC} (pin 16) to 12.5V ±0.5V. (Note: I_{CC} will be approximately 300mA during the programming procedure.)
   3. Address the word to be programmed through A_0 through A_6 using 0V to 0.5V as logical "0" and 2.4V to 5.0V as logical "1".
   4. Force 64 ±3mA into the output to be programmed to a "1". (Note: LIMIT THE OUTPUT VOLTAGE TO 20.0V MAX. PROGRAM ONE OUTPUT AT A TIME.)

      NOTE: V_{CC} and output programming pulse width should be 50ms (1.0 sec max.).
   5. Remove the programming current from the output and remove V_{CC}. (Do not exceed a 25% power on duty cycle during programming.)
   6. Repeat steps 2 through 5 until the addressed word is completely programmed.
   7. Repeat steps 2 through 6 until the device is completely programmed.

B. Fast Programming Procedure
   1. Steps 1 through 3 same as above in slow procedures.
   4. Force 64 ±3mA into the output, limited to 20.0V max, to be programmed to a "1" and monitor the voltage at the output pin. When the output voltage rises above 19.5V the bit is programmed. (Note: Unprogrammed outputs will be 18.7V or less. Typical Programming time is 10 millisec/bit.)
   5. Remove the current source and apply it to the next output, in the same word, to be programmed. (Note: Full power may be applied to the device for 1.0 sec continuously. Therefore, bits may be programmed until 1.0 sec has been accumulated. At that time, remove all power for 4.0 seconds, then continue programming.)
   6. Repeat steps 4 and 5 until the entire word is programmed.
   7. Repeat steps 2 through 6 until the device is fully programmed. The typical 82S26 or 82S29 can be programmed in less than one-half minute using the above procedure.

AC TEST FIGURE AND WAVEFORM



Ground Pins 13 and 14 when testing address-Output delays

SECTION 9
SIGNETICS SURE 883 PROGRAM

FOR DIGITAL DEVICES
BULLETIN 5001A

The Signetics SURE*/883 Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability of Signetics products. *These tests are made regularly at no extra cost to* the user and are performed in addition to the 40 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below for the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production and include 100% final production electrical tests. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed electrical test limits and conditions applicable to each subgroup are shown in the Electrical Characteristics table of the individual part type data sheets.

Tables IIIA, IIIB, and IIIC provide a complete process qualification and verification program in accordance with the conditions of MIL-STD-883, Group A, B and C tests. These tests are performed once in every 90 day manufacturing period, on representative devices from each standard production die process family and on each production package family. The representative circuits and packages selected are changed routinely, and the tests performed monitor and qualify all structurally similar devices produced by the same process and production during that period. A summary of these test results is available on request at the time of order placement.

All of the applicable Electrical Parameters of Table IIIA are performed at pretest on the Table IIIC samples. This provides the MIL-STD-883 electrical parameter and design verification Group A tests. *These tests are performed on representative circuit types from* every die process family type in manufacturing during this period.

Table IIIB consists of the package oriented qualification environmental stress tests of MIL-STD-883, Groups B and C. Representative samples from each package product family type are monitored and qualified every 90 day period by these tests. A common device is used as the die type for these package and assembly qualification tests.

Table IIIC consists of the die process oriented qualification electrical stress or operational tests at high temperature per MIL-STD-883, Groups B and C. Representative devices from each die process family are monitored and qualified every 90 day period by these tests. The package type is randomly selected as applicable.

An additional screening series is available at extra cost. Details are given in Table V, MIL-STD-883, method 5004, high reliability screening.

Table I — 100% Production Screen Tests

TEST	CONDITIONS
Preseal Visual	High Power — Low Power
Thermal Shock	Liquid to Liquid, 5 Cycles, 60 Seconds at 0°C, 60 Seconds at 100°C, transfer time 5 Seconds. (See Note 1.)
Centrifuge	Y_1 Axis; 30,000 g minimum, 1 minute. (See Note 1.)
Hermeticity	Gross leak test (Bubble Test). (See Note 1.)
Production Electrical Tests	

Table II — Signetics Acceptance Tests (See Notes 2 and 3)

SIGNETICS SUBGROUP	TEST	CONDITIONS	AQL	MIL-STD-105 INSPECTION LEVEL
A-1	Visual and Mechanical Inspection	MIL-STD-883 Method 2009	1.0%	II
A-2	DC Parameters	T_A = +25°C	1.0%	II
A-3	DC Parameters	T_A = +25°C	1.0%	II
A-4	DC Parameters	T_A = +125° C	1.0%	II
A-5	DC Parameters	T_A = −55°C	1.0%	II
A-6	AC Parameters	T_A = +25°C	1.0%	II

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* Systematic Uniformity and Reliability Evaluation

TABLE IIIA. MIL-STD-883 GROUP A ELECTRICAL TESTS

MIL-STD-883 GROUP A SUBGROUP	SIGNETICS SUBGROUP	TEST DESCRIPTION
A1	A-2, A-3	Static tests at 25°C
A2	A-4	Static tests at maximum rated operating temperature.
A3	A-5	Static tests at minimum rated operating temperature.
A4	A-6	Dynamic tests at 25°C,
A5	C 2, when applicable	Dynamic tests at maximum rated operating temperature.
A6	C 2, when applicable	Dynamic tests at minimum rated operating temperature.
A7	*	Functional tests at 25°C.
A8	A-4, A-5	Functional tests at maximum and minimum rated operating temperatures.
A9	A-6	Switching tests at 25°C.
A10	C 2, when applicable	Switching tests at maximum rated operating temperature.
A11	C-2, when applicable	Switching tests at minimum rated operating temperature.

TABLE IIIB. MIL-STD-883 GROUPS B AND C ENVIRONMENTAL TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
B_1	Physical Dimensions	2008	Test Condition A	15
B_2	Marking Permanency	2008	Test Condition B, Para. 3,2,1	4 devices/no failure
	Visual and Mechanical	2008	Test Condition B	1 device/no failure
	Bond Strength	2011	Test Condition D	15
B_3	Solderability	2003	Solder Temperature 260°C ±10°C	15
B_4	Lead Fatigue	2004	Test Condition B_2	15
	Hermeticity	1014	See Note 4	
	a. Fine		Test Condition A or B	
	b. Gross		Test Condition C	
C_1	Pre-Test Electrical Parameters		Signetics Subgroup A-3	
	Thermal Shock	1011	15 Cycles. Test Condition C, +150°C to -65°C	15
	Temperature Cycle	1010	10 Cycles. Test Condition C, 150°C to -65°C	
	Moisture Resistance	1004	Omit initial conditioning.	
	End Point Electrical Parameters		Signetics Subgroup A-3	
	FAILURE CRITERIA		Refer to Table IV.	
C_2	Pre-Test Electrical Parameters		Signetics Subgroup A-3	
	Mechanical Shock	2002	Test Condition B	15
	Vibration Variable Frequency	2007	Test Condition A	
	Constant Acceleration	2001	Test Condition E	
	End Point Electrical Parameters		Signetics Subgroup A-3	
	FAILURE CRITERIA		Refer to Table IV.	
C_3	Salt Atmosphere	1009	Test Condition A. Omit initial conditioning.	15
C_4	Pre-Test Electrical Parameters		Signetics Subgroup A-3	
	High Temperature Storage	1008	T_A = +150°C, t = 1000 hours	λ = 15
	End Point Electrical Parameters		Signetics Subgroup A-3	
	FAILURE CRITERIA		Refer to Table IV.	

TABLE IIIC. MIL-STD-883 GROUPS B AND C HIGH TEMPERATURE OPERATING LIFE TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
	Pre-Test and Design Verification Electrical Parameters		Table IIIA as applicable, data sheet groups A & C.	
B_5 & C_5	High Temperature Operating Life	1005	Test Condition D or E as applicable. T_A = +125°C or +85°C, per Part Data Sheet. t = 1000 hours.	λ = 10
	End Point Electrical Parameters		Signetics Subgroup A-3	
	FAILURE CRITERIA		Refer to Table IV.	

*Signetics performs a truth table test.

Table IV — Signetics Failure Criteria

TEST	"1" Input Current	"1" Output Voltage	"0" Input Current	"0" Output Voltage	Expansion Node Current
LIMITS	Data Sheet Limits and: 10X Initial Value for DTL 5X Initial Value for TTL	Data Sheet Limits and: ±20% Initial Value	Data Sheet Limits ±20% Initial Value	Data Sheet Limits and: ±0.1V	Data Sheet Limits and: ±20% Initial Value

Optional High Reliability Screening

To maximize reliability in critical application, the Optional High Reliability Screening of Table V provides for three levels of 100% screening per MIL-STD-883, Method 5004 at extra cost. This series eliminates the necessity for special specification, minimizes cost and provides the shortest possible delivery time. This series is applied after the normal Group A acceptance test. Circuits subjected to this Preconditioning Series are clearly distinguishable from standard products in the following ways:

1. Individual serial number on each circuit (Class A only).
2. The first letters of a part number are either RA, RB, or RC.
   RA = Class A
   RB = Class B
   RC = Class C
   i.e., RA8880J = 100% screening of Table V, Class A.
3. Individual device variables parametric test data is supplied with each shipment (Class A only).

Consult your local representative for price information. Device types should be specified with the appropriate letter prefixes.

Notes:

1. Not applicable to solid molded packaged devices.
2. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
3. Detailed tests, conditions, and limits applicable to each subgroup are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table. See Table IIIA for the corresponding Group A tests of MIL-STD-883.
4. The Hermeticity tests are not employed for solid molded packages.
5. Class B and Class C may be subjected to thermal shock as an alternate.
6. The test sequence of fine and gross leak may be reversed when fluorocarbons are utilized for gross leak.
7. The individual MIL-STD-883 Test Methods are, in many cases designed to "stand alone" as a sole screen or sole Group B environmental sampling test. But since 5004 specifies a screening series or flow, some of the measurements, etc., specified in an individual Test Method are not intended to be applicable in the screening series.

TABLE V — MIL-STD-883 METHOD 5004, HIGH RELIABILITY SCREENING

TEST	MIL-STD-883 METHOD	CLASS A	CLASS B	CLASS C	CLARIFICATIONS (See Note 7)
Internal Visual (preseal)	2010.1	Cond. A	Cond. B	Cond. B	Test Condition A, Paragraph 3.1.1.7, a, delete the words "and parameter".
Stabilization Bake	1008 (24 hours)	Cond. C	Cond. C	Cond. C	Condition C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements at this point.
Thermal Shock	1011	Cond C	Not required. NOTE 5	Not required. NOTE 5	Cond. C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection at this point.
Temperature Cycling	1010	Cond. C	Cond. C NOTE 5	Cond. C NOTE 5	(150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection, no hermeticity tests at this point.
Mechanical Shock	2002, Y1 plane only	Cond. B	Not Required	Not Required	No electrical measurements at this point.
Centrifuge	2001	Cond. E Y2 then Y1 plane	Cond. E Y1 plane	Cond. E Y1 plane	
Hermeticity A. Fine Leak B. Gross Leak	1014, Note 6 (Hermetic devices only)	Cond. A or B Cond. C	Cond. A or B Cond. C	Cond. A or B Cond. C	
Critical Electrical Parameters	Signetics Subgroup A-3	Read and Record	Not Required	Not Required	
Burn In Test	1015, T_A = +125°C	240 hours Cond. D or E (as applicable)	168 hours Cond. D or E (as applicable)	Not Required	
Critical Electrical Parameters	Signetics Subgroup A 3	Read and Record	Not Required	Not Required	
Signetics FAILURE CRITERIA		Table IV	Not Required	Not Required	
Reverse Bias Burn In	1015, T_A = +150°C t = 72 hours	Cond A or C	Not Required	Not Required	Required only when specified in the applicable procurement document. Signetics standard burn-in (above) includes reverse bias of unused junctions.
Final Electrical Test	Perform go no go measurements of Signetics Subgroup A Parameters	Signetics Subgroups A 2, A 4, A 5, A 6, Functional tests, truth table when applicable	Signetics Subgroups A 2, A 3, A 6, Functional tests, truth table when applicable	Signetics Subgroups A 2, A 3 Functional tests, truth table when applicable	
Radiographic Inspection	2012	Yes	Not Required	Not Required	
External Visual	2009	Yes	Yes	Yes	

SECTION 10
CUSTOMER ORDERING INFORMATION

N8205Y - CB175	ASCII-TO-EBCDIC, EBCDIC-TO-ASCII
N8204Y - CB504	ASCII-TO-EBCDIC CODE CONVERTER
N8204Y - CB505	EBCDIC-TO-ASCII CODE CONVERTER

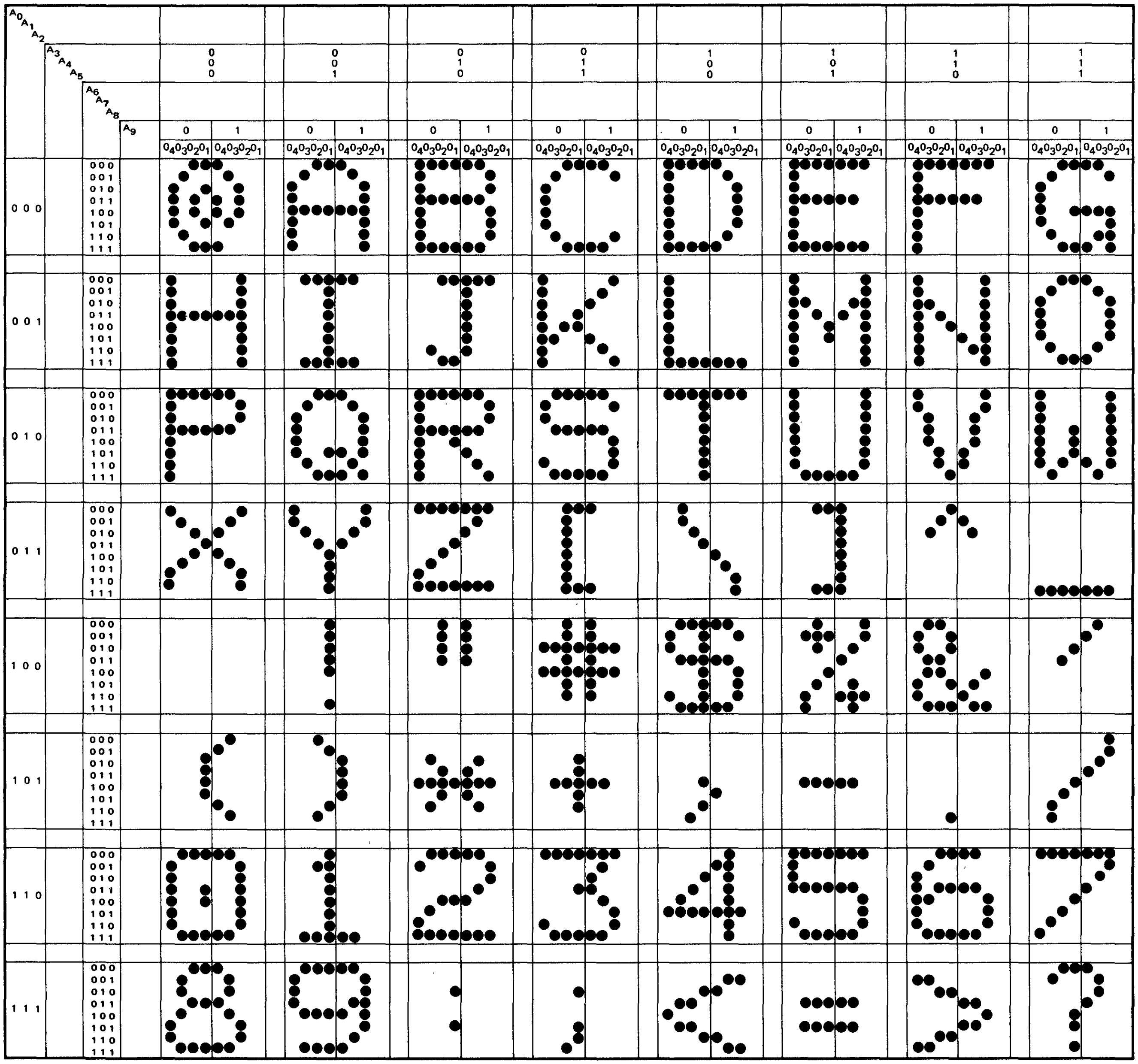
ASCII (ADDRESS) TO EBCDIC (DATA) 8205 — CB175 FIRST HALF
8204 — CB504

0 00000000	1 00000001	2 00000010	3 00000011	128 00100000	129 00100001	130 00100010	131 00100011
4 00110111	5 00101101	6 00101110	7 00101111	132 00100100	133 00010101	134 00000110	135 00010111
8 00010110	9 00000101	10 00100101	11 00001011	136 00101000	137 00101001	138 00101010	139 00101011
12 00001100	13 00001101	14 00001110	15 00001111	140 00101100	141 00001001	142 00001010	143 00011011
16 00010000	17 00010001	18 00010010	19 00010011	144 00110000	145 00110001	146 00011010	147 00110011
20 00111100	21 00111101	22 00110010	23 00100110	148 00110100	149 00110101	150 00110110	151 00001000
24 00011000	25 00011001	26 00111111	27 00100111	152 00111000	153 00111001	154 00111010	155 00111011
28 00011100	29 00011101	30 00011110	31 00011111	156 00000100	157 00010100	158 00111110	159 11100001
32 01000000	33 01001111	34 01111111	35 01111011	160 01000001	161 01000010	162 01000011	163 01000100
36 01011011	37 01101100	38 01010000	39 01111101	164 01000101	165 01000110	166 01000111	167 01001000
40 01001101	41 01011101	42 01011100	43 01001110	168 01001001	169 01010001	170 01010010	171 01010011
44 01101011	45 01100000	46 01001011	47 01100001	172 01010100	173 01010101	174 01010110	175 01010111
48 11110000	49 11110001	50 11110010	51 11110011	176 01011000	177 01011001	178 01100010	179 01100011
52 11110100	53 11110101	54 11110110	55 11110111	180 01100100	181 01100101	182 01100110	183 01100111
56 11111000	57 11111001	58 01111010	59 01011110	184 01101000	185 01101001	186 01110000	187 01110001
60 01001100	61 01111110	62 01101110	63 01101111	188 01110010	189 01110011	190 01110100	191 01110101
64 01111100	65 11000001	66 11000010	67 11000011	192 01110110	193 01110111	194 01111000	195 10000000
68 11000100	69 11000101	70 11000110	71 11000111	196 10001010	197 10001011	198 10001100	199 10001101
72 11001000	73 11001001	74 11010001	75 11010010	200 10001110	201 10001111	202 10010000	203 10011010
76 11010011	77 11010100	78 11010101	79 11010110	204 10011011	205 10011100	206 10011101	207 10011110
80 11010111	81 11011000	82 11011001	83 11100010	208 10011111	209 10100000	210 10101010	211 10101011
84 11100011	85 11100100	86 11100101	87 11100110	212 10101100	213 10101101	214 10101110	215 10101111
88 11100111	89 11101000	90 11101001	91 01001010	216 10110000	217 10110001	218 10110010	219 10110011
92 11100000	93 01011010	94 01011111	95 01101101	220 10110100	221 10110101	222 10110110	223 10110111
96 01111001	97 10000001	98 10000010	99 10000011	224 10111000	225 10111001	226 10111010	227 10111011
100 10000100	101 10000101	102 10000110	103 10000111	228 10111100	229 10111101	230 10111110	231 10111111
104 10001000	105 10001001	106 10010001	107 10010010	232 11001010	233 11001011	234 11001100	235 11001101
108 10010011	109 10010100	110 10010101	111 10010110	236 11001110	237 11001111	238 11011010	239 11011011
112 10010111	113 10011000	114 10011001	115 10100010	240 11011100	241 11011101	242 11011110	243 11011111
116 10100011	117 10100100	118 10100101	119 10100110	244 11101010	245 11101011	246 11101100	247 11101101
120 10100111	121 10101000	122 10101001	123 11000000	248 11101110	249 11101111	250 11111010	251 11111011
124 01101010	125 11010000	126 10100001	127 00000111	252 11111100	253 11111101	254 11111110	255 11111111

EBCDIC (ADDRESS) TO ASCII (DATA) 8205 — CB175 SECOND HALF
8204 — CB505

256 00000000	257 00000001	258 00000010	259 00000011	384 11000011	385 01100001	386 01100010	387 01100011
260 10011100	261 00001001	262 10000110	263 01111111	388 01100100	389 01100101	390 01100110	391 01100111
264 10010111	265 10001101	266 10001110	267 00001011	392 01101000	393 01101001	394 11000100	395 11000101
268 00001100	269 00001101	270 00001110	271 00001111	396 11000110	397 11000111	398 11001000	399 11001001
272 00010000	273 00010001	274 00010010	275 00010011	400 11001010	401 11001010	402 01101011	403 01101100
276 10011101	277 10000101	278 00001000	279 10000111	404 01101101	405 01101110	406 01101111	407 01110000
280 00011000	281 00011001	282 10010010	283 10001111	408 01110001	409 01110010	410 11001011	411 11001100
284 00011100	285 00011101	286 00011110	287 00011111	412 11001101	413 11001110	414 11001111	415 11010000
288 10000000	289 10000001	290 10000010	291 10000011	416 11010001	417 01111110	418 01110011	419 01110100
292 10000100	293 00001010	294 00010111	295 00011011	420 01110101	421 01110110	422 01110111	423 01111000
296 10001000	297 10001001	298 10001010	299 10001011	424 01111001	425 01111010	426 11010010	427 11010011
300 10001100	301 00000101	302 00000110	303 00000111	428 11010100	429 11010101	430 11010110	431 11010111
304 10010000	305 10010001	306 00010110	307 10010011	432 11011000	433 11011001	434 11011010	435 11011011
308 10010100	309 10010101	310 10010110	311 00000100	436 11011100	437 11011101	438 11011110	439 11011111
312 10011000	313 10011001	314 10011010	315 10011011	440 11100000	441 11100001	442 11100010	443 11100011
316 00010100	317 00010101	318 10011110	319 00011010	444 11100100	445 11100101	446 11100110	447 11100111
320 00100000	321 10100000	322 10100001	323 10100010	448 01111011	449 01000001	450 01000010	451 01000011
324 10100011	325 10100100	326 10100101	327 10100110	452 01000100	453 01000101	454 01000110	455 01000111
328 10100111	329 10101000	330 01011011	331 00101110	456 01001000	457 01001001	458 11101000	459 11101001
332 00111100	333 00101000	334 00101011	335 00100001	460 11101010	461 11101011	462 11101100	463 11101101
336 00100110	337 10101001	338 10101010	339 10101011	464 01111101	465 01001010	466 01001011	467 01001100
340 10101100	341 10101101	342 10101110	343 10101111	468 01001101	469 01001110	470 01001111	471 01010000
344 10110000	345 10110001	346 01011101	347 00100100	472 01010001	473 01010010	474 11101110	475 11101111
348 00101010	349 00101001	350 00111011	351 01011110	476 11110000	477 11110001	478 11110010	479 11110011
352 00101101	353 00101111	354 10110010	355 10110011	480 01011100	481 10011111	482 01010011	483 01010100
356 10110100	357 10110101	358 10110110	359 10110111	484 01010101	485 01010110	486 01010111	487 01011000
360 10111000	361 10111001	362 01111100	363 00101100	488 01011001	489 01011010	490 11110100	491 11110101
364 00100101	365 01011111	366 00111110	367 00111111	492 11110110	493 11110111	494 11111000	495 11111001
368 10111010	369 10111011	370 10111100	371 10111101	496 00110000	497 00110001	498 00110010	499 00110011
372 10111110	373 10111111	374 11000000	375 11000001	500 00110100	501 00110101	502 00110110	503 00110111
376 11000010	377 01100000	378 00111010	379 00100011	504 00111000	505 00111001	506 11111010	507 11111011
380 01000000	381 00100111	382 00111101	383 00100010	508 11111100	509 11111101	510 11111110	511 11111111

N8228I - CD162 PATTERN
USASC II ROW CHARACTER GENERATOR



PUNCHED CARD PROGRAM INPUT FOR 8204 & 8205

The customer may specify the content of the ROM either by filling out the accompanying form or by using punched cards. He should note that:

1. "Zero" levels on data out lines are defined as low.
2. Address bit A_0 is the least significant address bit. (See 8204 and 8205 data sheet)

Punched Card Data Input - Data to program the 8205 and the 8204 can be supplied in punched card-format. The format for the data is shown in Figure 1. Each data word is preceded by an address word which identifies its position in memory. Figure 2 shows the deck format for the 8204 256 x 8 bit ROM. For the 8204 the first card in the deck contains the part number and it is immediately followed by up to 40 alphanumeric characters of customer supplied information used to identify the part. The 64 customer data cards follow immediately. Figure 3 shows the deck format for the 8205 512 x 8 ROM. For the 8205 the first card in the deck contains the part number and it is immediately followed by up to 40 alphanumeric characters of customer supplied information used to identify the part. 128 data cards follow immediately. The left-most digit in the data word corresponds to output O_8 and the right-most digit to output O_1.

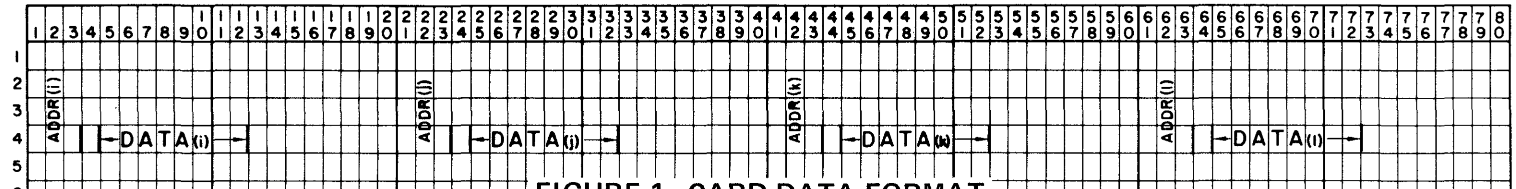


FIGURE 1. CARD DATA FORMAT

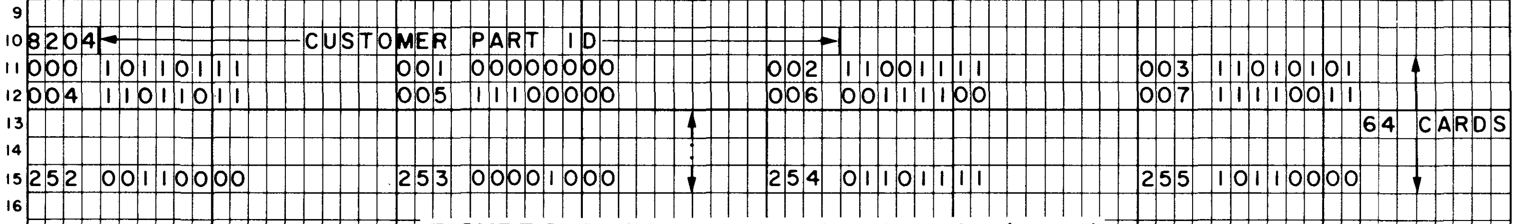


FIGURE 2. DECK FORMAT FOR 8204 ROM (256x8)

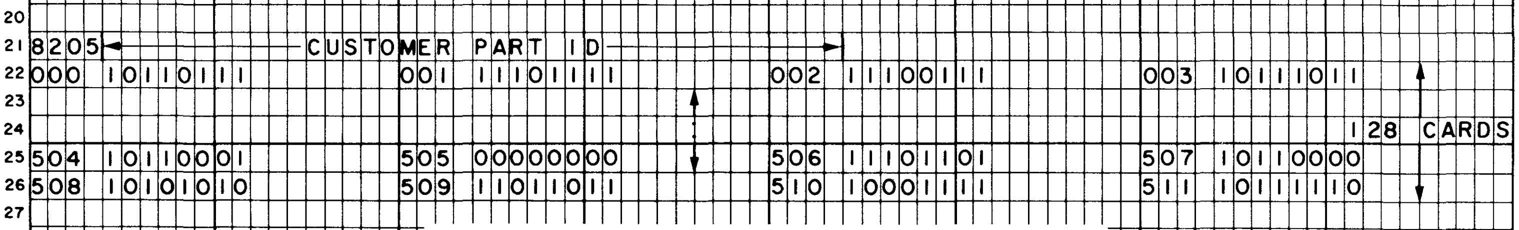


FIGURE 3. DECK FORMAT FOR 8205 ROM (512x8)

Punched card data to program can be transmitted directly to Signetics. Data information to program the ROM requires 128 80-column IBM punched cards per 4096 bit device and 64 punched cards per 256 bit device.

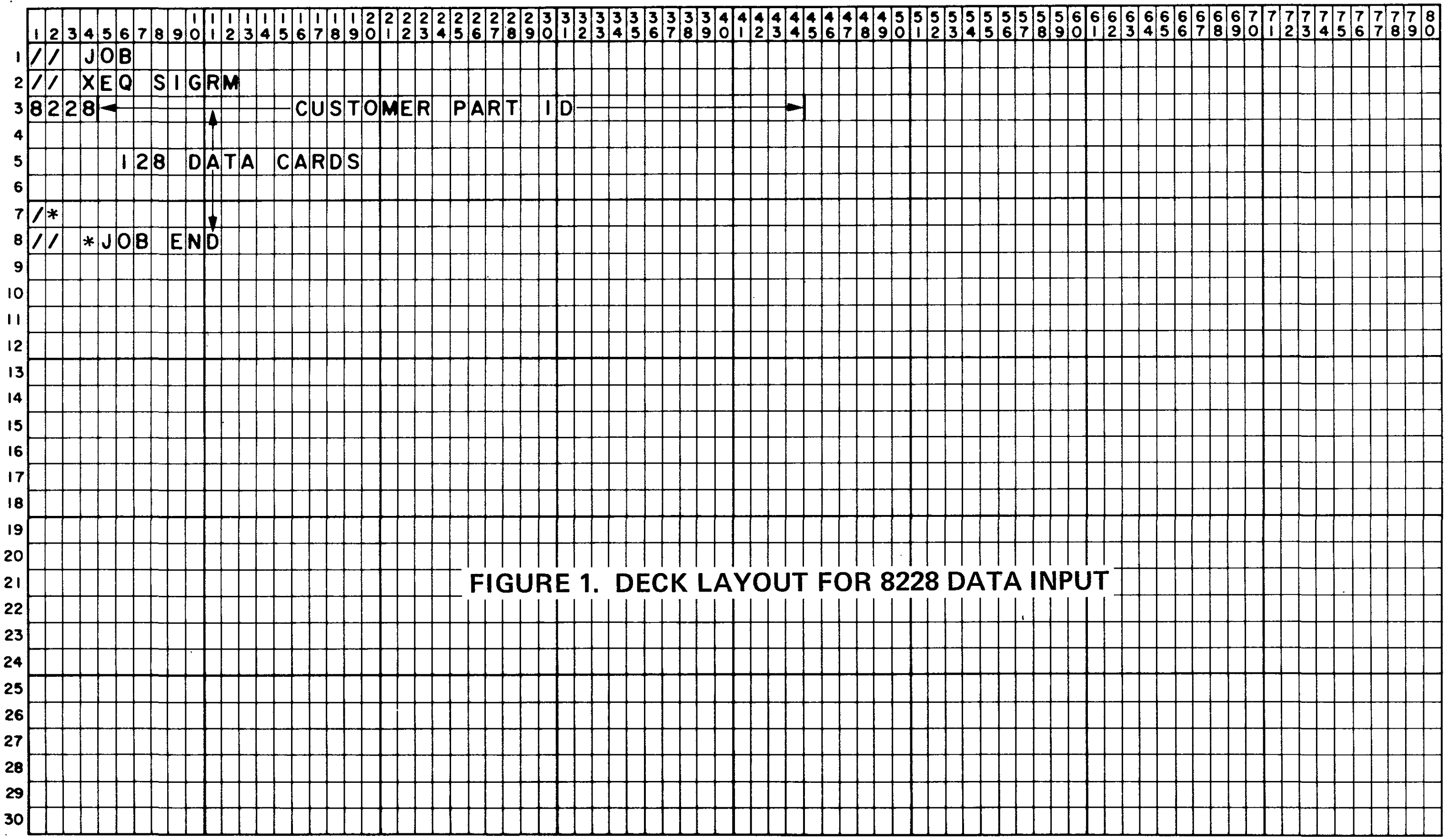
Input Deck Format

For each 4096 bit ROM, the customer should prepare an input card deck as shown in Figure 1. The first two cards should be punched as shown and placed at the start of the deck. The third card should contain "8228" in the first four columns. In the next 40 positions, the customer should fill in his own part identification. These first three cards are then followed by 128 data cards. Immediately following are two cards to terminate the computer run. These should be punched by the customer.

Data Cards

Figure 2 shows the layout used in the data cards. Each data card specifies eight addresses and the four bits of data associated with these addresses. Address (i) tells the computer what position to assign Data (i) to etc. Immediately under this, a typical layout for the first two and the last data cards is shown.

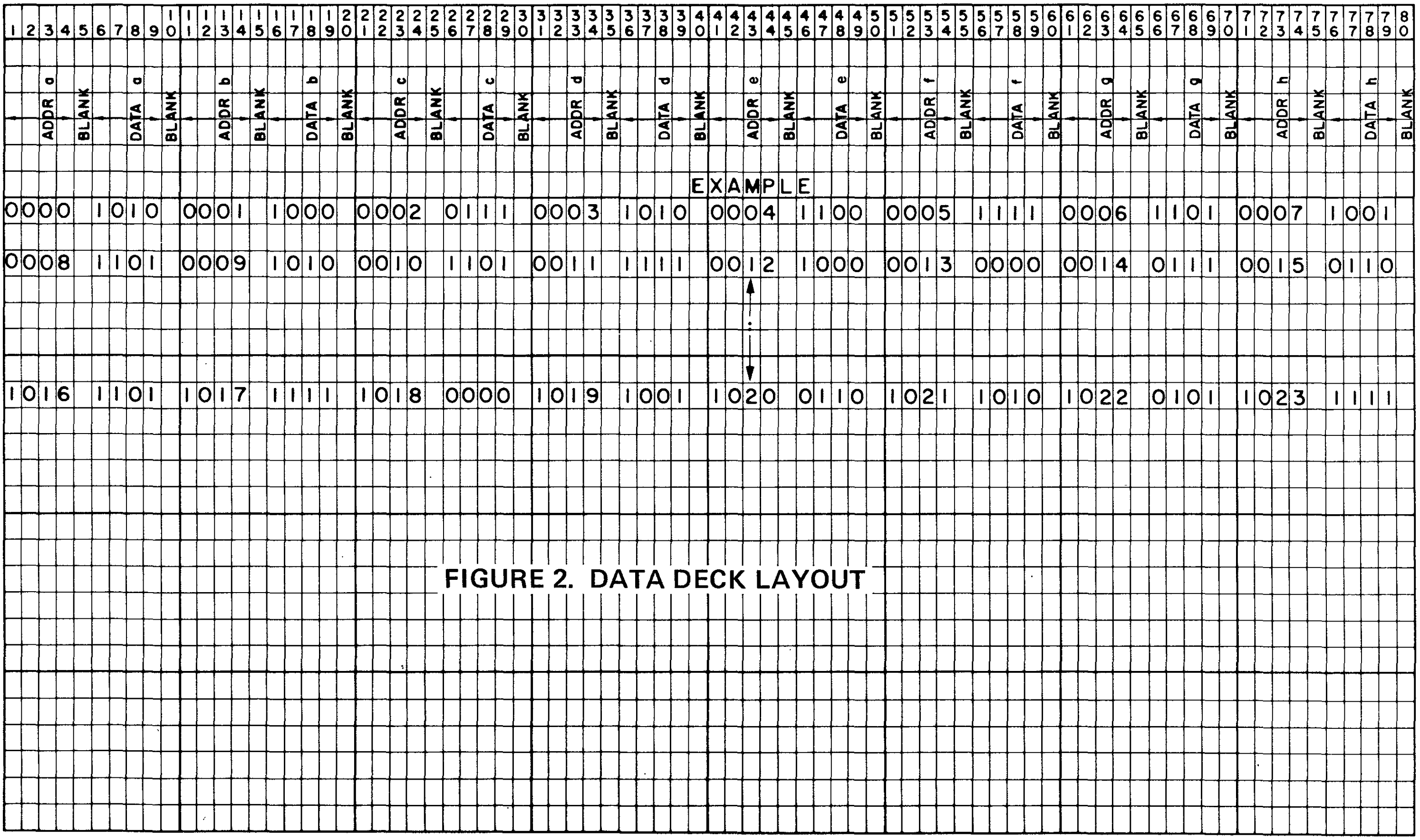
INPUT CARD



```
1  //  JOB
2  //  XEQ SIGRM
3  8228<------CUSTOMER PART ID------->
4
5       128 DATA CARDS
6
7  /*
8  //  *JOB END
```

FIGURE 1. DECK LAYOUT FOR 8228 DATA INPUT

DATA CARDS



EXAMPLE

Row	ADDR a	DATA a	ADDR b	DATA b	ADDR c	DATA c	ADDR d	DATA d	ADDR e	DATA e	ADDR f	DATA f	ADDR g	DATA g	ADDR h	DATA h
7	0000	1010	0001	1000	0002	0111	0003	1010	0004	1100	0005	1111	0006	1101	0007	1001
9	0008	1101	0009	1010	0010	1101	0011	1111	0012	1000	0013	0000	0014	0111	0015	0110
14	1016	1101	1017	1111	1018	0000	1019	1001	1020	0110	1021	1010	1022	0101	1023	1111

FIGURE 2. DATA DECK LAYOUT

(8204,8205)

2048/4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDERING BLANK

CUSTOMER: ______________________

P.O. NO.: ______________________

YOUR PART NO.: ______________________

DATE: ______________________

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: ______________________

S.D. NO.: ______________________

DATE RECEIVED: ______________________

Note: For 256 x 8 Use This Page Only

Word	OUTPUT								Word	OUTPUT								Word	OUTPUT								Word	OUTPUT							
	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0									64									128									192								
1									65									129									193								
2									66									130									194								
3									67									131									195								
4									68									132									196								
5									69									133									197								
6									70									134									198								
7									71									135									199								
8									72									136									200								
9									73									137									201								
10									74									138									202								
11									75									139									203								
12									76									140									204								
13									77									141									205								
14									78									142									206								
15									79									143									207								
16									80									144									208								
17									81									145									209								
18									82									146									210								
19									83									147									211								
20									84									148									212								
21									85									149									213								
22									86									150									214								
23									87									151									215								
24									88									152									216								

25									89									153									217								
26									90									154									218								
27									91									155									219								
28									92									156									220								
29									93									157									221								
30									94									158									222								
31									95									159									223								
32									96									160									224								
33									97									161									225								
34									98									162									226								
35									99									163									227								
36									100									164									228								
37									101									165									229								
38									102									166									230								
39									103									167									231								
40									104									168									232								
41									105									169									233								
42									106									170									234								
43									107									171									235								
44									108									172									236								
45									109									173									237								
46									110									174									238								
47									111									175									239								
48									112									176									240								
49									113									177									241								
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52									116									180									244								
53									117									181									245								
54									118									182									246								
55									119									183									247								
56									120									184									248								
57									121									185									249								
58									122									186									250								
59									123									187									251								
60									124									188									252								
61									125									189									253								
62									126									190									254								
63									127									191									255								

(8204,8205)
2048/4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDERING BLANK

CUSTOMER: ____________________

P.O. NO.: ____________________

YOUR PART NO.: ____________________

DATE: ____________________

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: ____________________

S.D. NO.: ____________________

DATE RECEIVED: ____________________

Note: For 256 x 8 Use Previous Page Only

Word	OUTPUT								Word	OUTPUT								Word	OUTPUT								Word	OUTPUT							
	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
256									320									384									448								
257									321									385									449								
258									322									386									450								
259									323									387									451								
260									324									388									452								
261									325									389									453								
262									326									390									454								
263									327									391									455								
264									328									392									456								
265									329									393									457								
266									330									394									458								
267									331									395									459								
268									332									396									460								
269									333									397									461								
270									334									398									462								
271									335									399									463								
272									336									400									464								
273									337									401									465								
274									338									402									466								
275									339									403									467								
276									340									404									468								
277									341									405									469								
278									342									406									470								
279									343									407									471								
280									344									408									472								

281									345									409									473								
282									346									410									474								
283									347									411									475								
284									348									412									476								
285									349									413									477								
286									350									414									478								
287									351									415									479								
288									352									416									480								
289									353									417									481								
290									354									418									482								
291									355									419									483								
292									356									420									484								
293									357									421									485								
294									358									422									486								
295									359									423									487								
296									360									424									488								
297									361									425									489								
298									362									426									490								
299									363									427									491								
300									364									428									492								
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303									367									431									495								
304									368									432									496								
305									369									433									497								
306									370									434									498								
307									371									435									499								
308									372									436									500								
309									373									437									501								
310									374									438									502								
311									375									439									503								
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314									378									442									506								
315									379									443									507								
316									380									444									508								
317									381									445									509								
318									382									446									510								
319									383									447									511								

(8223,8224)

CB (XXX) 256 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: ____________________

P.O. NO.: ____________________

YOUR PART NO.: ____________________

DATE: ____________________

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: ____________________

S.D. NO.: ____________________

DATE RECEIVED: ____________________

WORD	INPUTS						OUTPUTS							
	A_4	A_3	A_2	A_1	A_0	ENABLE	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
ALL	X	X	X	X	X	1	1	1	1	1	1	1	1	1

(82S26) (82S29)
CB (XXXX) 1024 BIT READ ONLY MEMORY TRUTH TABLE/ORDER BLANK

CUSTOMER: ____________________

P.O. NO.: ____________________

YOUR PART NO.: ____________________

DATE: ____________________

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: ____________________

S.D. NO.: ____________________

DATE RECEIVED: ____________________

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
0					64					128					192				
1					65					129					193				
2					66					130					194				
3					67					131					195				
4					68					132					196				
5					69					133					197				
6					70					134					198				
7					71					135					199				
8					72					136					200				
9					73					137					201				
10					74					138					202				
11					75					139					203				
12					76					140					204				
13					77					141					205				
14					78					142					206				
15					79					143					207				
16					80					144					208				
17					81					145					209				
18					82					146					210				
19					83					147					211				
20					84					148					212				
21					85					149					213				
22					86					150					214				
23					87					151					215				
24					88					152					216				
25					89					153					217				

26					90					154					218				
27					91					155					219				
28					92					156					220				
29					93					157					221				
30					94					158					222				
31					95					159					223				
32					96					160					224				
33					97					161					225				
34					98					162					226				
35					99					163					227				
36					100					164					228				
37					101					165					229				
38					102					166					230				
39					103					167					231				
40					104					168					232				
41					105					169					233				
42					106					170					234				
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44					108					172					236				
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57					121					185					249				
58					122					186					250				
59					123					187					251				
60					124					188					252				
61					125					189					253				
62					126					190					254				
63					127					191					255				

(8228)
4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDER BLANK

CUSTOMER: ____________________

P.O. NO.: ____________________

YOUR PART NO.: ____________________

DATE: ____________________

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: ____________________

S.D. NO.: ____________________

DATE RECEIVED: ____________________

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
0					70					140					210				
1					71					141					211				
2					72					142					212				
3					73					143					213				
4					74					144					214				
5					75					145					215				
6					76					146					216				
7					77					147					217				
8					78					148					218				
9					79					149					219				
10					80					150					220				
11					81					151					221				
12					82					152					222				
13					83					153					223				
14					84					154					224				
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16					86					156					226				
17					87					157					227				
18					88					158					228				
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22					92					162					232				
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24					94					164					234				
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26					96					166					236				
27					97					167					237				
28					98					168					238				

29					99					169					239				
30					100					170					240				
31					101					171					241				
32					102					172					242				
33					103					173					243				
34					104					174					244				
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41					111					181					251				
42					112					182					252				
43					113					183					253				
44					114					184					254				
45					115					185					255				
46					116					186					256				
47					117					187					257				
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62					132					202					272				
63					133					203					273				
64					134					204					274				
65					135					205					275				
66					136					206					276				
67					137					207					277				
68					138					208					278				
69					139					209					279				

(8228)

4096 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: ________________

P.O. NO.: ________________

YOUR PART NO.: ________________

DATE: ________________

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: ________________

S.D. NO.: ________________

DATE RECEIVED: ________________

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
280					350					420					490				
281					351					421					491				
282					352					422					492				
283					353					423					493				
284					354					424					494				
285					355					425					495				
286					356					426					496				
287					357					427					497				
288					358					428					498				
289					359					429					499				
290					360					430					500				
291					361					431					501				
292					362					432					502				
293					363					433					503				
294					364					434					504				
295					365					435					505				
296					366					436					506				
297					367					437					507				
298					368					438					508				
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301					371					441					511				
302					372					442					512				
303					373					443					513				
304					374					444					514				
305					375					445					515				
306					376					446					516				
307					377					447					517				
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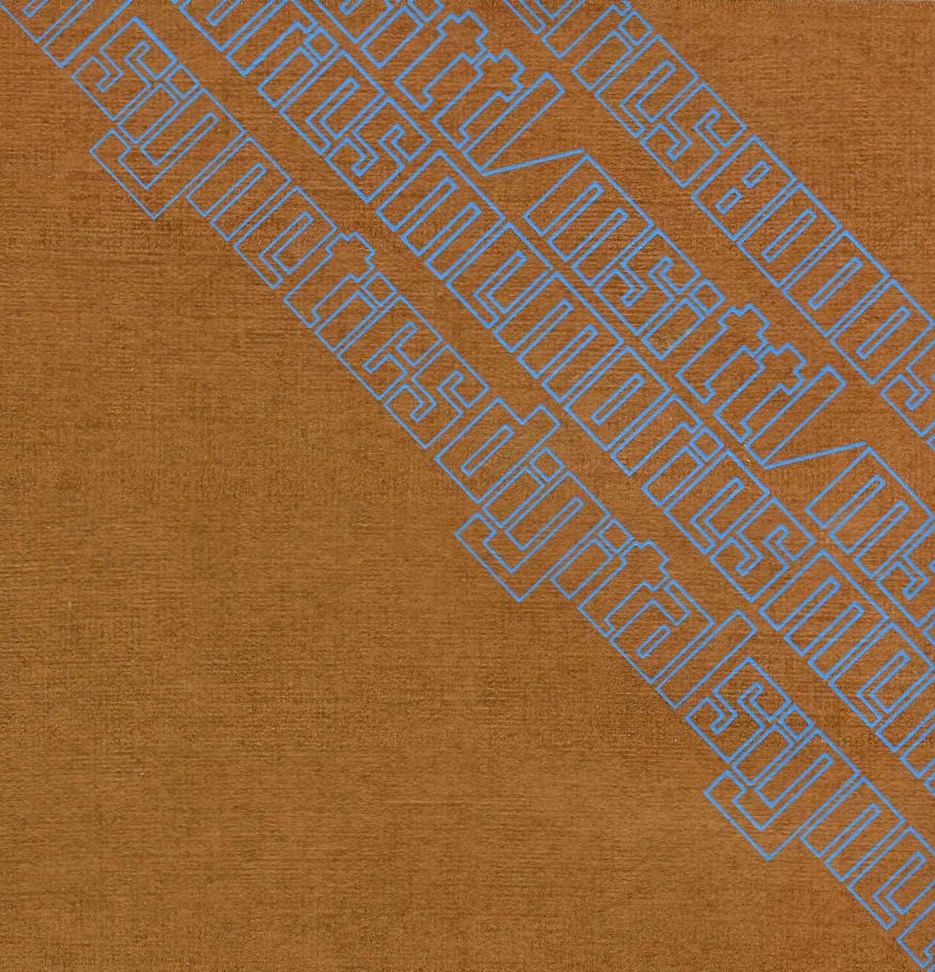

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